Protecting against Statistical Ineffective Fault Attacks

Joan Daemen, Christoph Dobraunig, Maria Eichlseder, Hannes Gross, Florian Mendel and Robert Primas

CHES 2020

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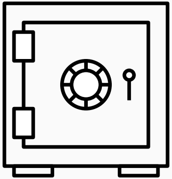

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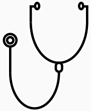
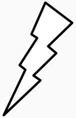
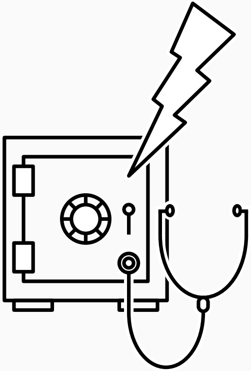


Power Analysis



Fault Attacks



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- Statistical Ineffective Fault Attacks (SIFA) were first presented at CHES2018:
  - Work against block ciphers, AEAD, etc. . .
  - Circumvent redundancy/infection countermeasures
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    - SIFA can additionally circumvent (higher-order) masking/TI
- Proposed countermeasures at the time:
    - Error correction
    - Hiding
    - Self destruction

Motivation cont.

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  - Rather expensive (masking!)
  - How much error correction is necessary?
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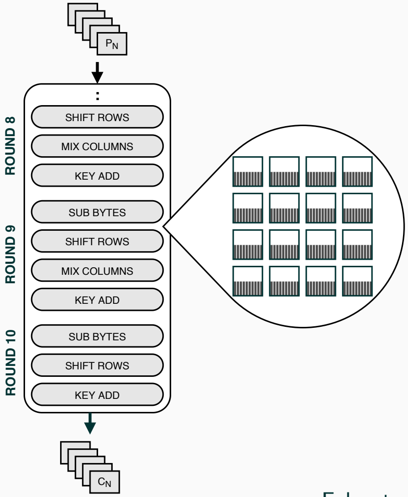
  - How much error correction is necessary?
  - What about DFA?
- We propose efficient SIFA countermeasure strategies:
  - "Careful" combination of redundancy with masking
  - Low overhead for lightweight schemes
  - Moderate overhead for "bulky" schemes like AES

Statistical Fault Attacks on AES-128

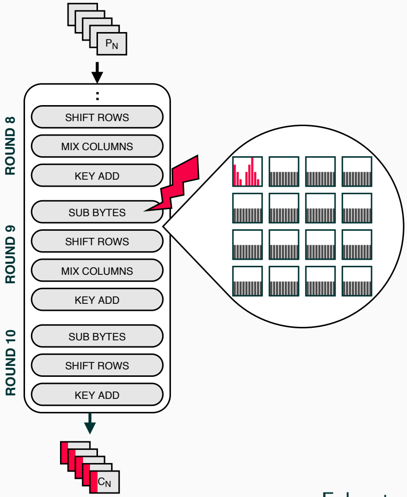
- AES is a PRP:
  - Distribution of ciphertext bytes is uniform
  - (Also after only 9 rounds)



Fuhr et al. [Fuh+13]

Statistical Fault Attacks on AES-128

- Assume fault that disturbs distribution of one state byte in round 9
  - Stuck-at, bitflip, random, etc.
  - Attacker does not need to know the caused bias
  - 4 ciphertext bytes are affected



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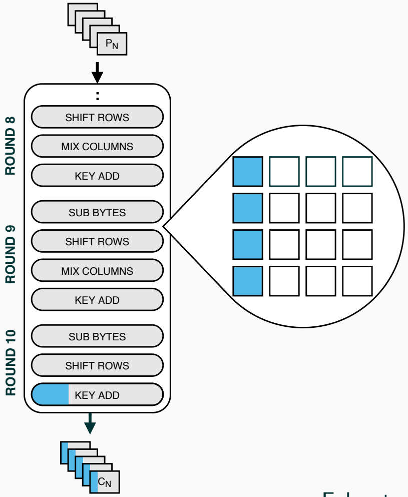

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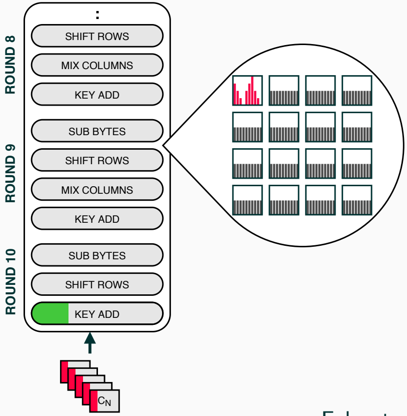

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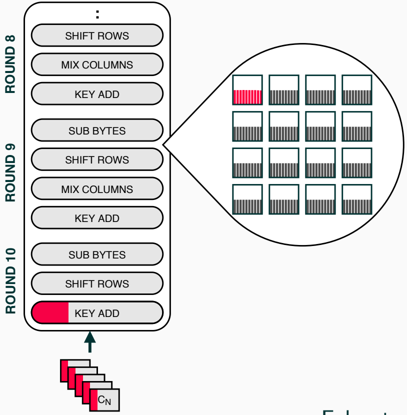

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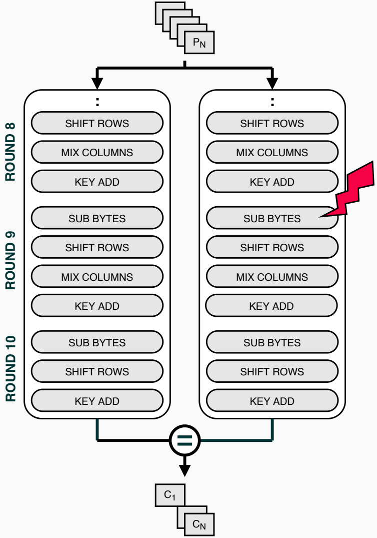

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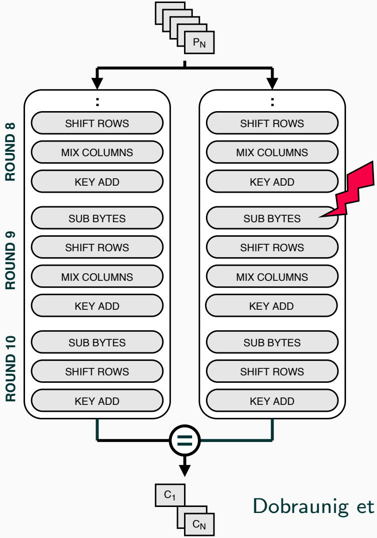

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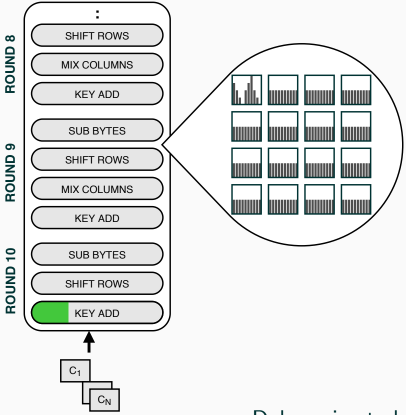

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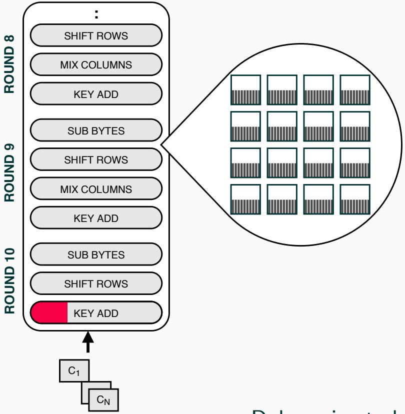

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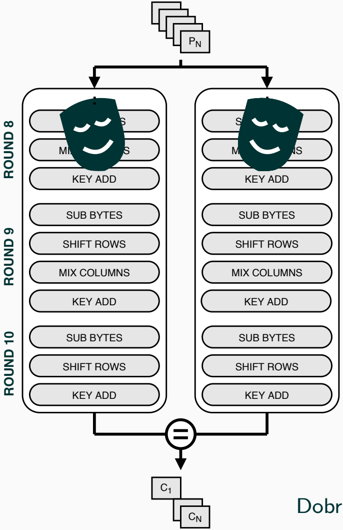

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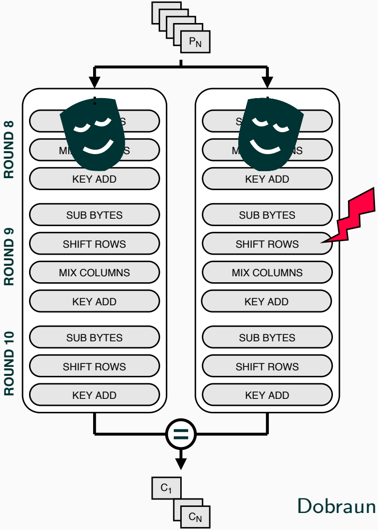

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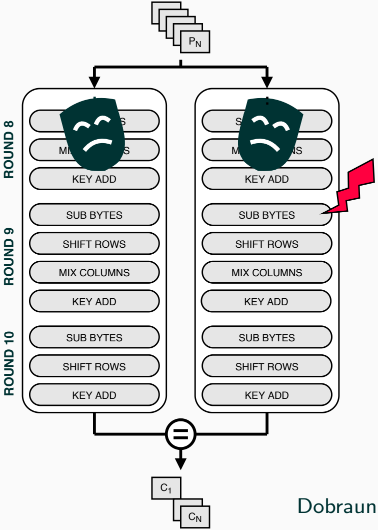

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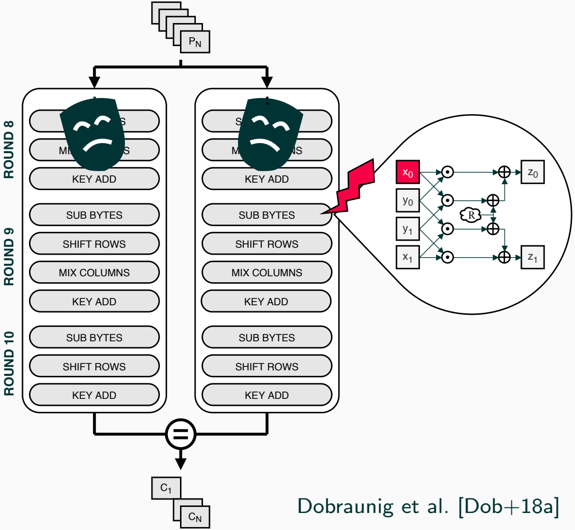

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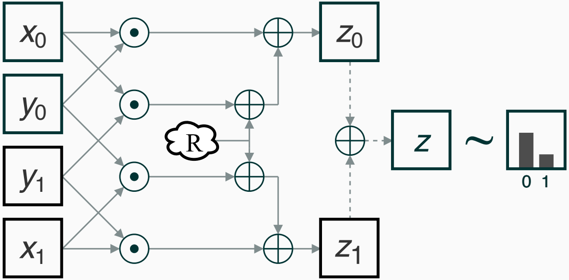
Statistical Ineffective Fault Attacks on AES-128

- Masked AND-gate
- Naturally, when x and y are uniform then z has bias towards 0



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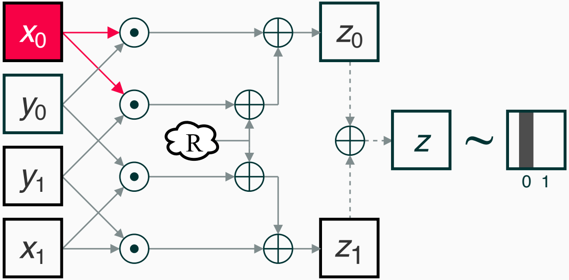

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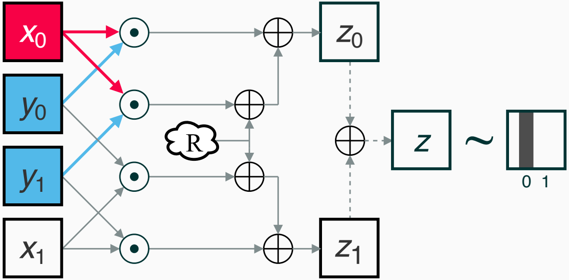

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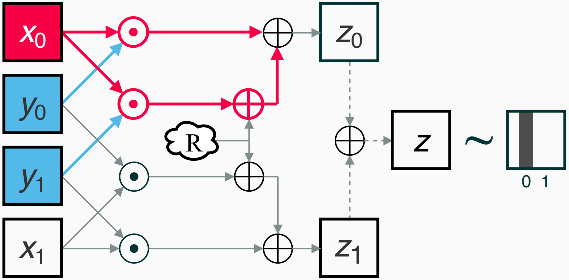

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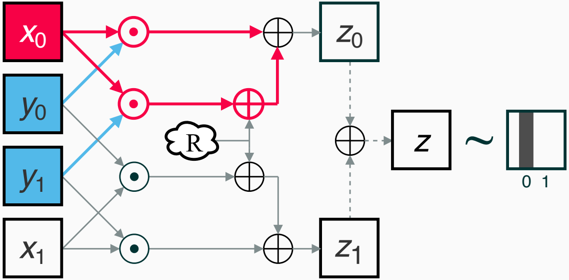
- Fault is ineffective iff native value y is zero

  $\Rightarrow$ "Dangerous fault"



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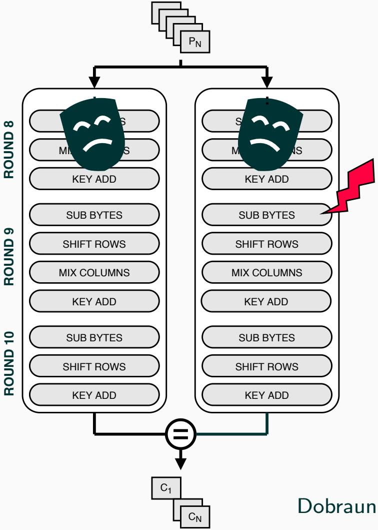

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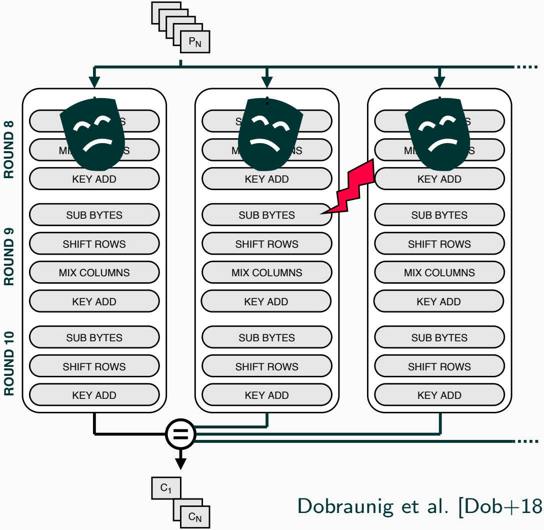

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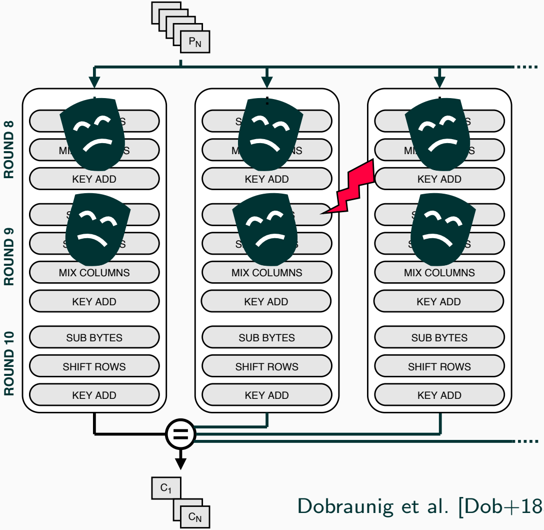

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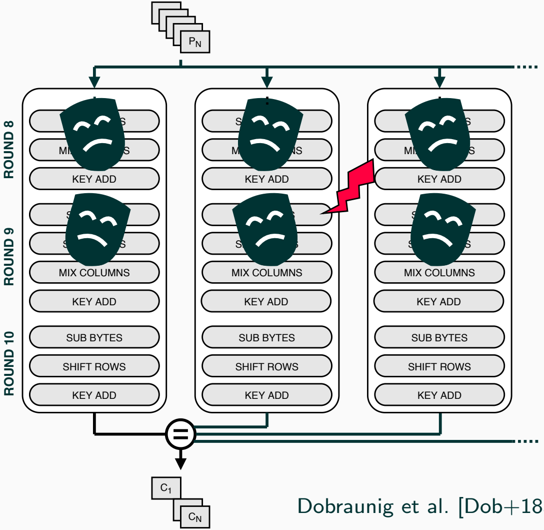
⇒ We now show how to counteract SIFA using masking + redundancy . . .



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- Splitting is done recursively until we have basic circuits:
  - Only consist of simple operations such as addition/multiplication

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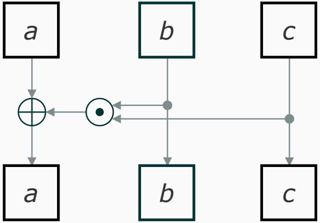

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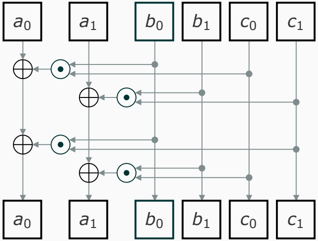
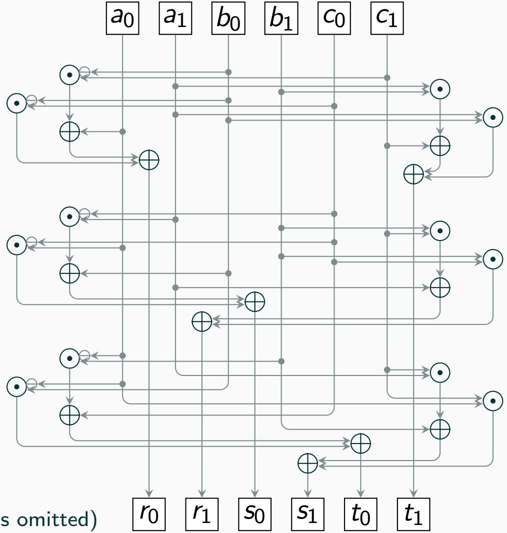


Case study: SIFA on Masked Chi-3 S-box



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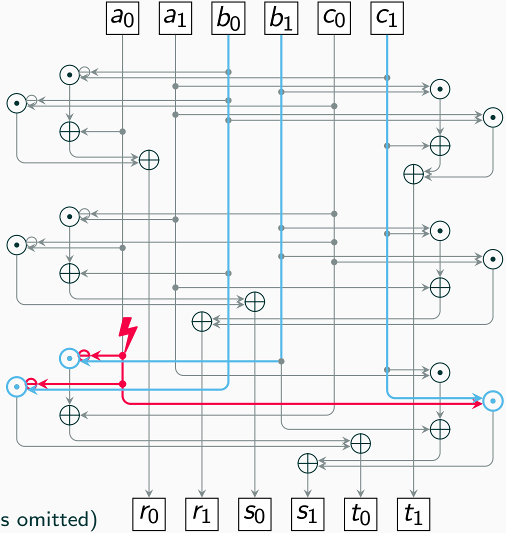

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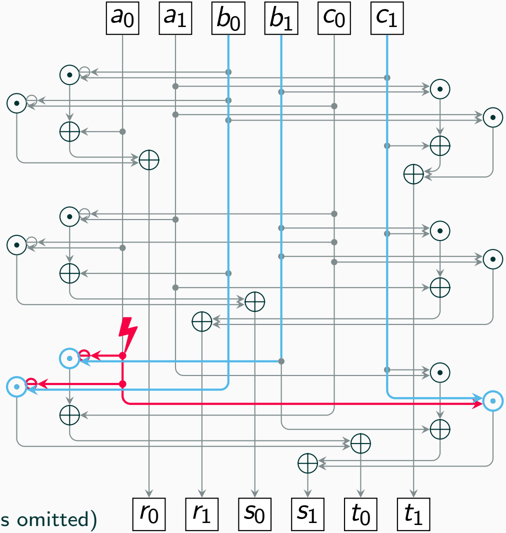

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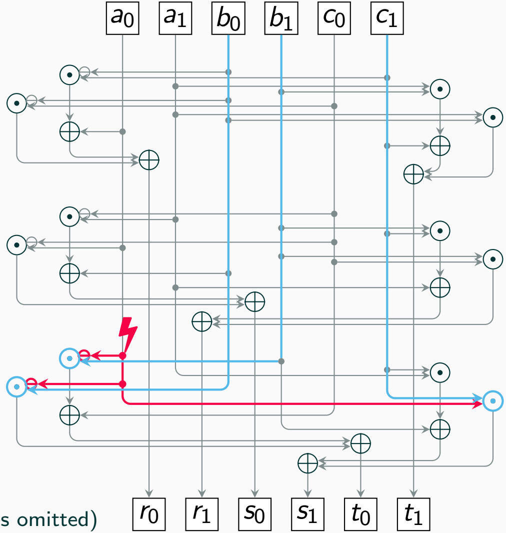
  - Bias at S-box output



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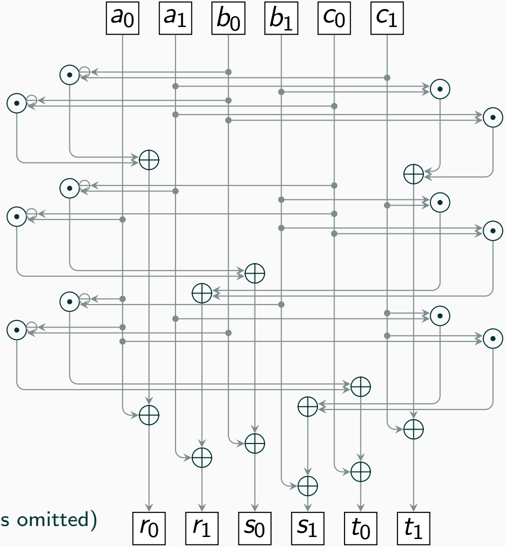

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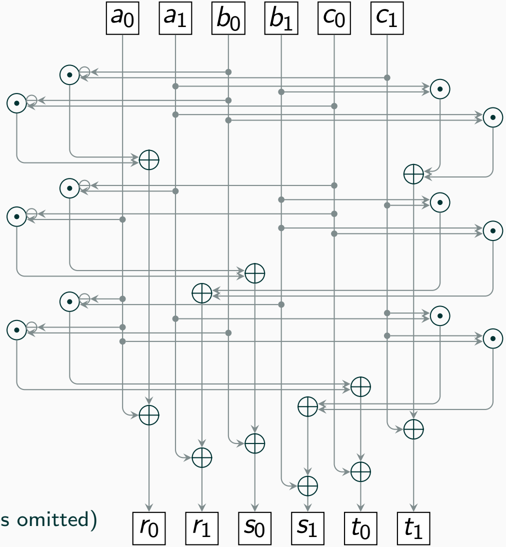

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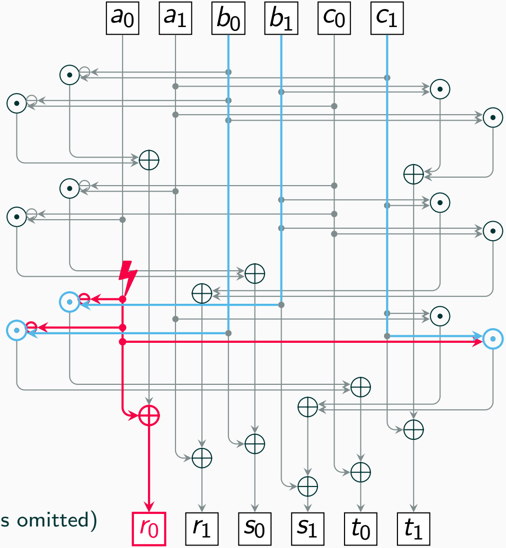

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- What about larger S-boxes like in AES?
  - Here we can use the Toffoli gate for bigger fields

AES S-box using Incomplete Permutation Basic Circuits

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- Replace all $F(2^n)$ multiplications by Toffoli gates operating in $F(2^n)$, using additional inputs that are set to zero

AES S-box using Incomplete Permutation Basic Circuits

- Inputs:
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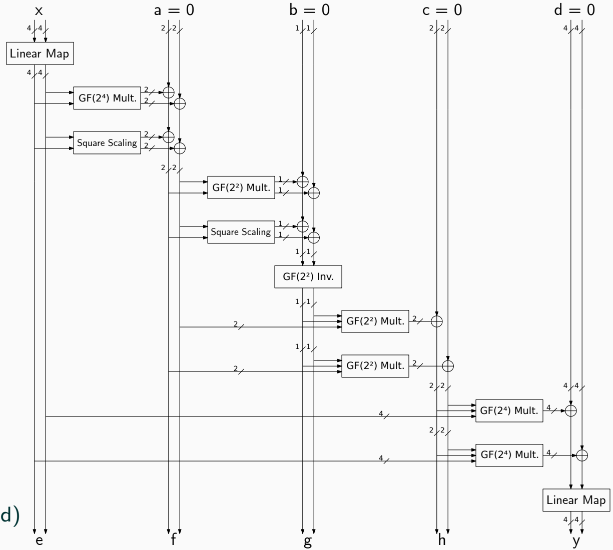
  - a, b, c, d (18-bits)



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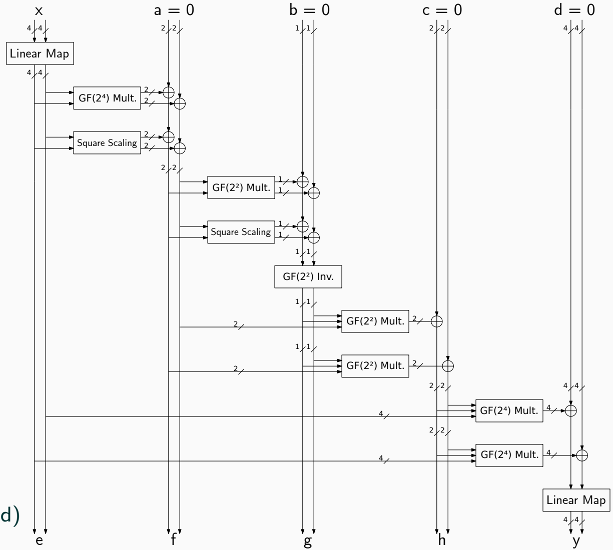

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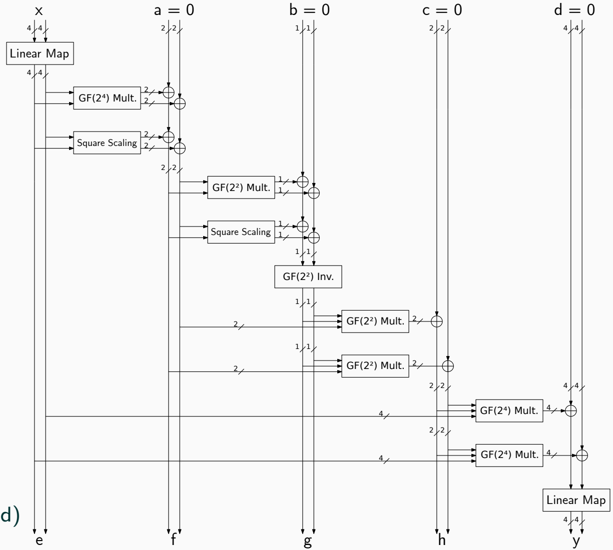

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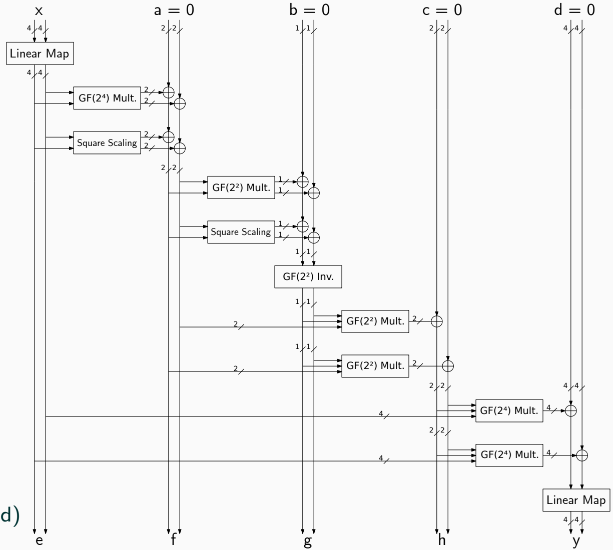

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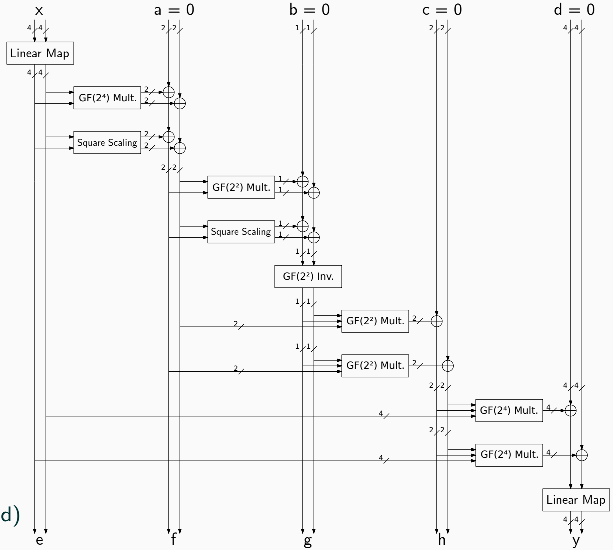

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- Discuss additional implementation aspects for SW/HW
- Present an alternative countermeasure strategy
  - Based on fine-grained redundancy checks
  - Can protect against multi-fault SIFA (but then not so efficient)

Final Remarks

In the paper we:

- Give a complete description of single-fault SIFA resistant (masked) AES S-box
- Discuss additional implementation aspects for SW/HW
- Present an alternative countermeasure strategy
    - Based on fine-grained redundancy checks
    - Can protect against multi-fault SIFA (but then not so efficient)

Side-note: SIFA protection also possible on mode-level (NIST LWC):

- DryGASCON, ISAP

Thank you!

Protecting against Statistical Ineffective Fault Attacks

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CHES 2020

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