Parallelizable Delegation from LWE

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Delegating RAM Computation

Delegating RAM Computation

Verifier **V**

Delegating RAM Computation

Prover **P**

M, x

Verifier **V**

Delegating RAM Computation

Prover **P**

y = M(x)

M, x

Verifier **V**

Delegating RAM Computation

Prover **P**

$y = M(x)$

M, x

$\longleftarrow$

$\longrightarrow$

y, π

Verifier **V**

Delegating RAM Computation

Prover **P**

y = M(x)

M, x

y, π

Verifier **V**

Completeness:

- If y = M(x),
  π convinces **V**.

Delegating RAM Computation

Prover **P**

y = M(x)

M, x

y, π

Verifier **V**

Completeness:

- If y = M(x), π convinces **V**.

Soundness:

- If y != M(x), PPT **P*** **cannot generate** a convincing π.

Delegating RAM Computation

Prover **P**

$y = M(x)$

M, x

y, π

Verifier **V**

Completeness:

- If $y = M(x)$, π convinces **V**.

Soundness:

- If $y \ne M(x)$, PPT **P*** **cannot generate** a convincing π.

Succinctness:

- $|\pi|$ and runtime of **V** are at most **polylog(T)** where $T = \mathrm{Time}_M(x)$.

Delegating RAM Computation

Prover **P**

y = M(x)

M, x

y, π

Verifier **V**

Ignoring poly(λ) terms

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- If y = M(x), π convinces **V**.

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Delegating RAM Computation

Prover **P**

$y = M(x)$

Verifier **V**

M, x ←

→ y, π

Completeness:

- If $y = M(x)$, π convinces **V**.

Soundness:

- If $y \mathrel{!}= M(x)$, PPT **P*** **cannot generate** a convincing π.

Succinctness:

- $|\pi|$ and runtime of **V** are at most **polylog(T)** where $T = \mathrm{Time}_M(x)$.

Delegating RAM Computation

CRS

Prover **P**

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M, x

←

→

y, π

Verifier **V**

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Delegating RAM Computatio

|CRS| <= polylog(T)

CRS

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y, π

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What does the prover do?

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Wall-clock time

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Wall-clock time

0 —————————— **T**

Compute M(x)

What does the prover do?

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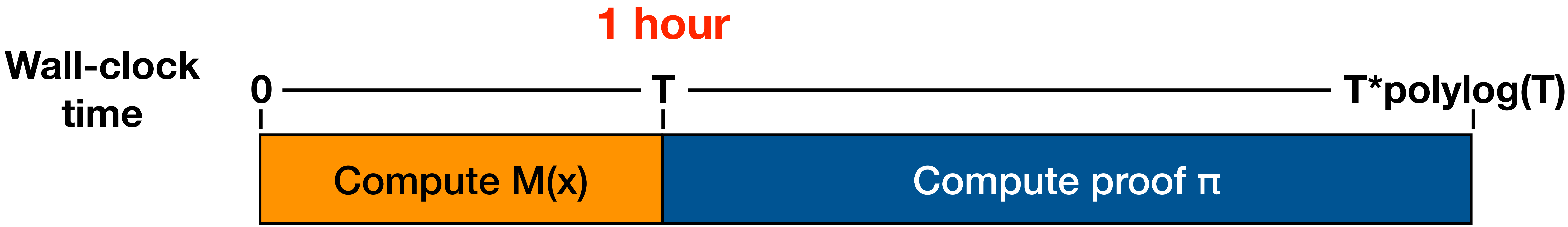

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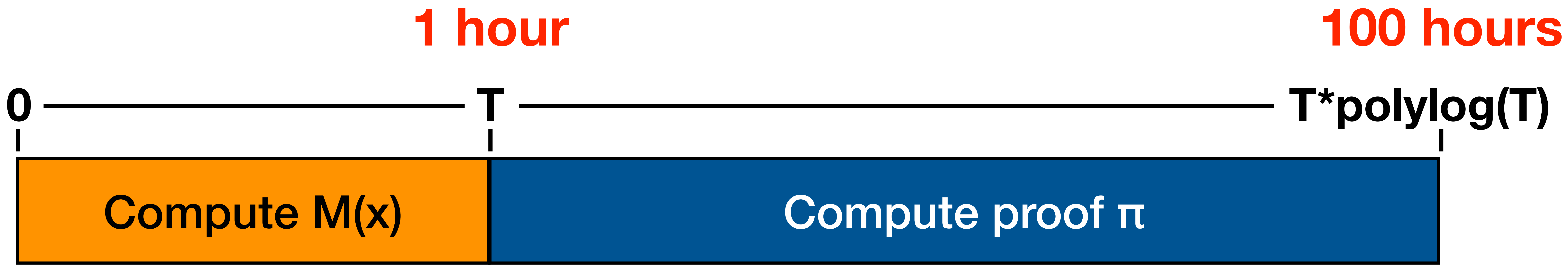

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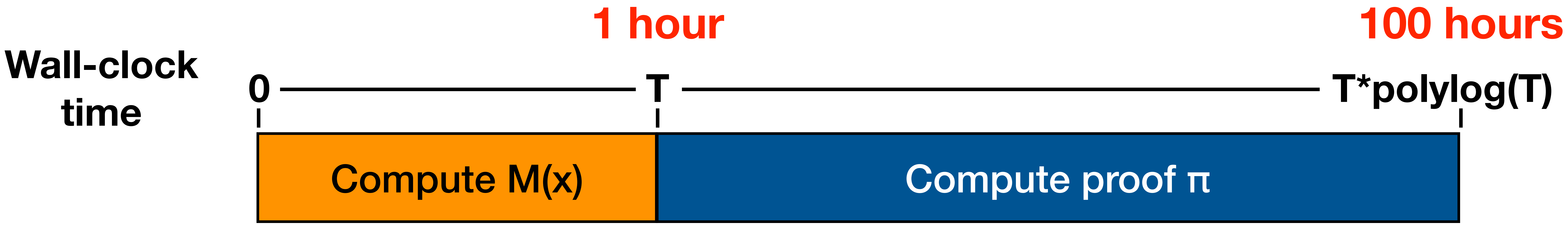
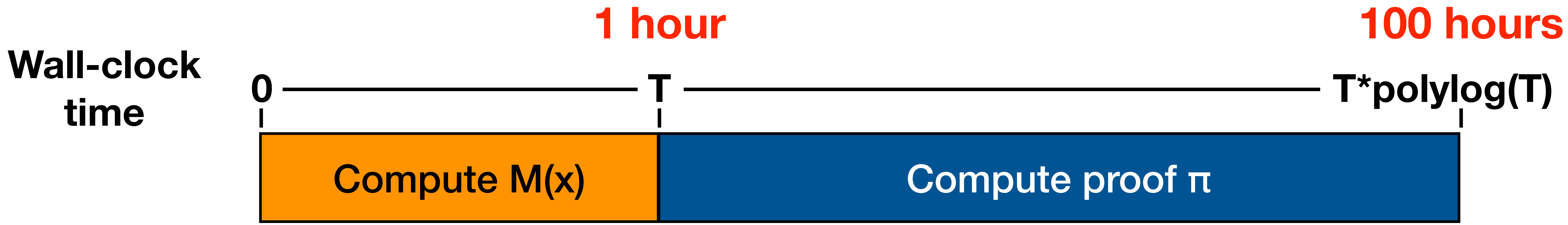


Quasi-linear T*polylog(T) prover efficiency:

What does the prover do?



Quasi-linear T*polylog(T) prover efficiency:

- from **ROM** or **SNARKs** [M94, BS05, BCCT13].

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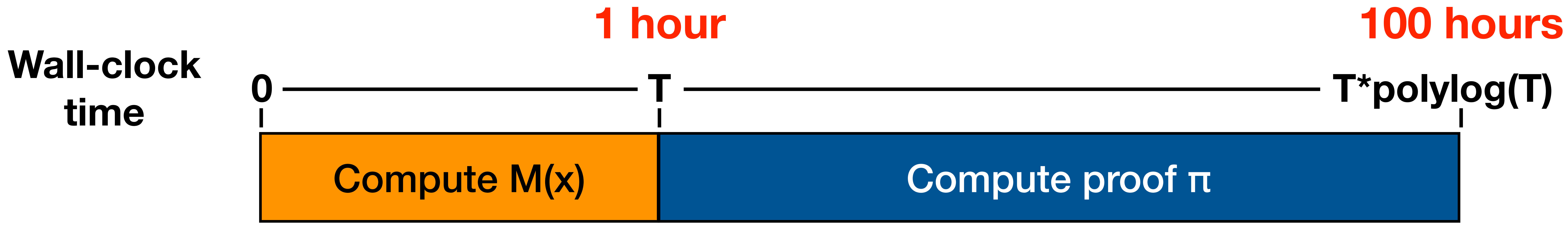
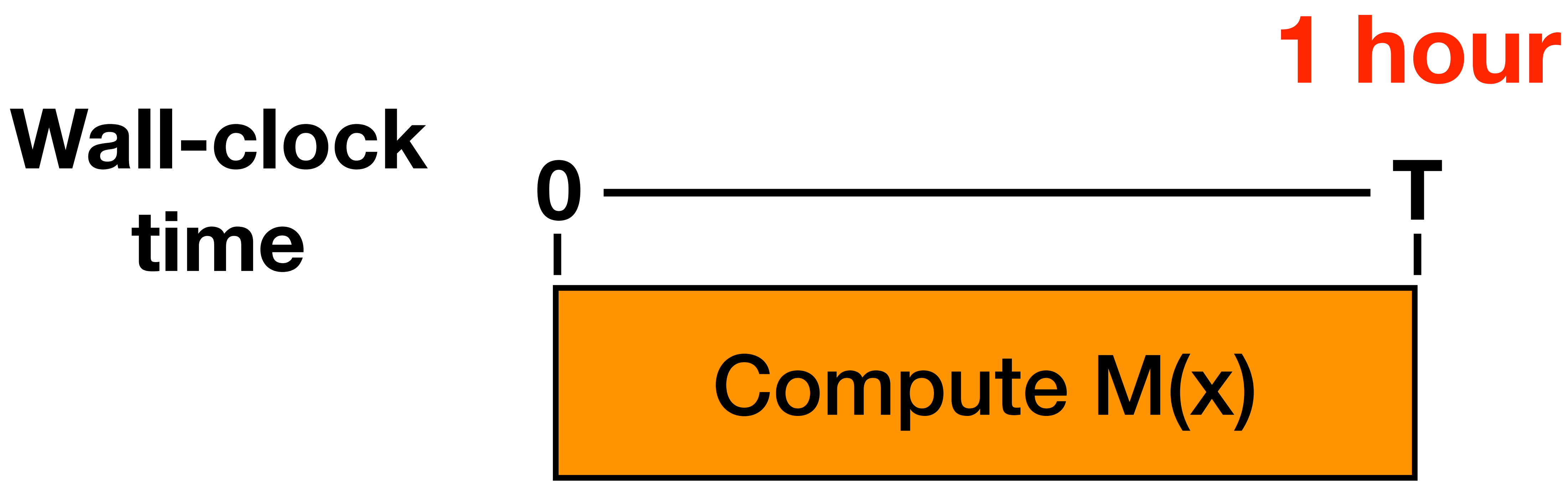


Quasi-linear T*polylog(T) prover efficiency:

- from **ROM** or **SNARKs** [M94, BS05, BCCT13].
- from **LWE** [CJJ21].

SPARG:
Parallelizable Delegation for RAM



SPARG:
Parallelizable Delegation for RAM

Succinct Parallelizable Argument

Wall-clock time

1 hour

0 ——— **T**

Compute M(x)

SPARG:
Parallelizable Delegation for RAM

1 hour

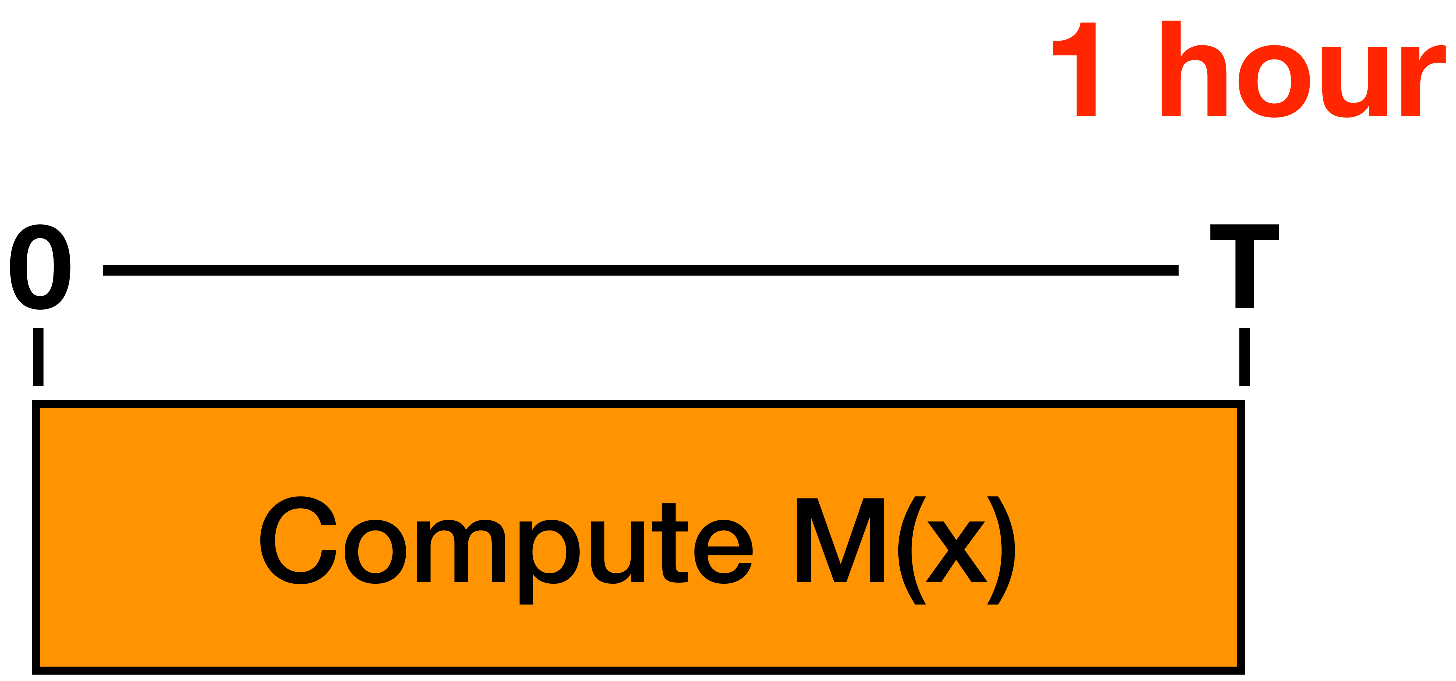
Wall-clock time

0 —————— **T**

Compute M(x)

SPARG:
Parallelizable Delegation for RAM

Wall-clock time



Compute the proof
in parallel
to the computation

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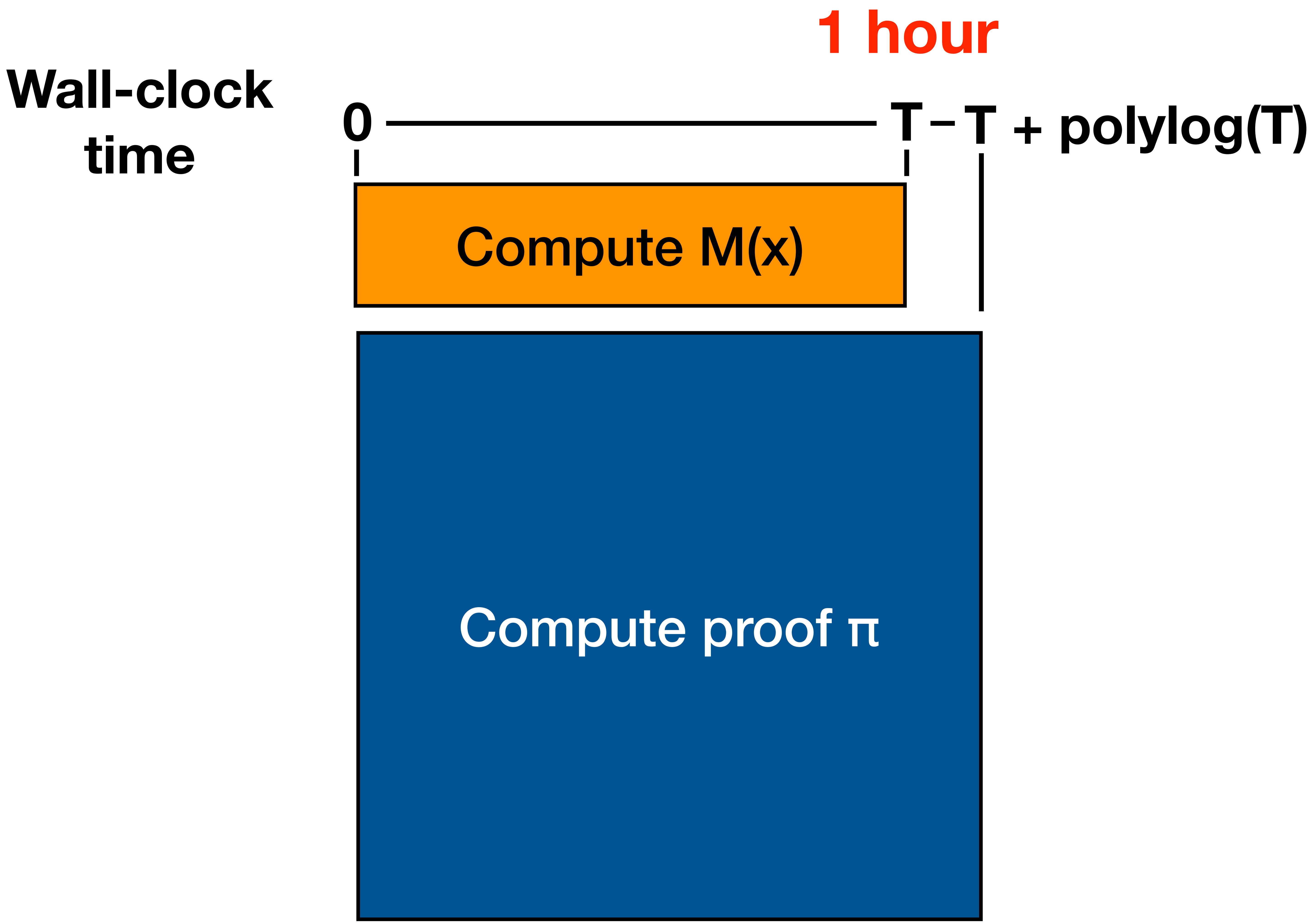

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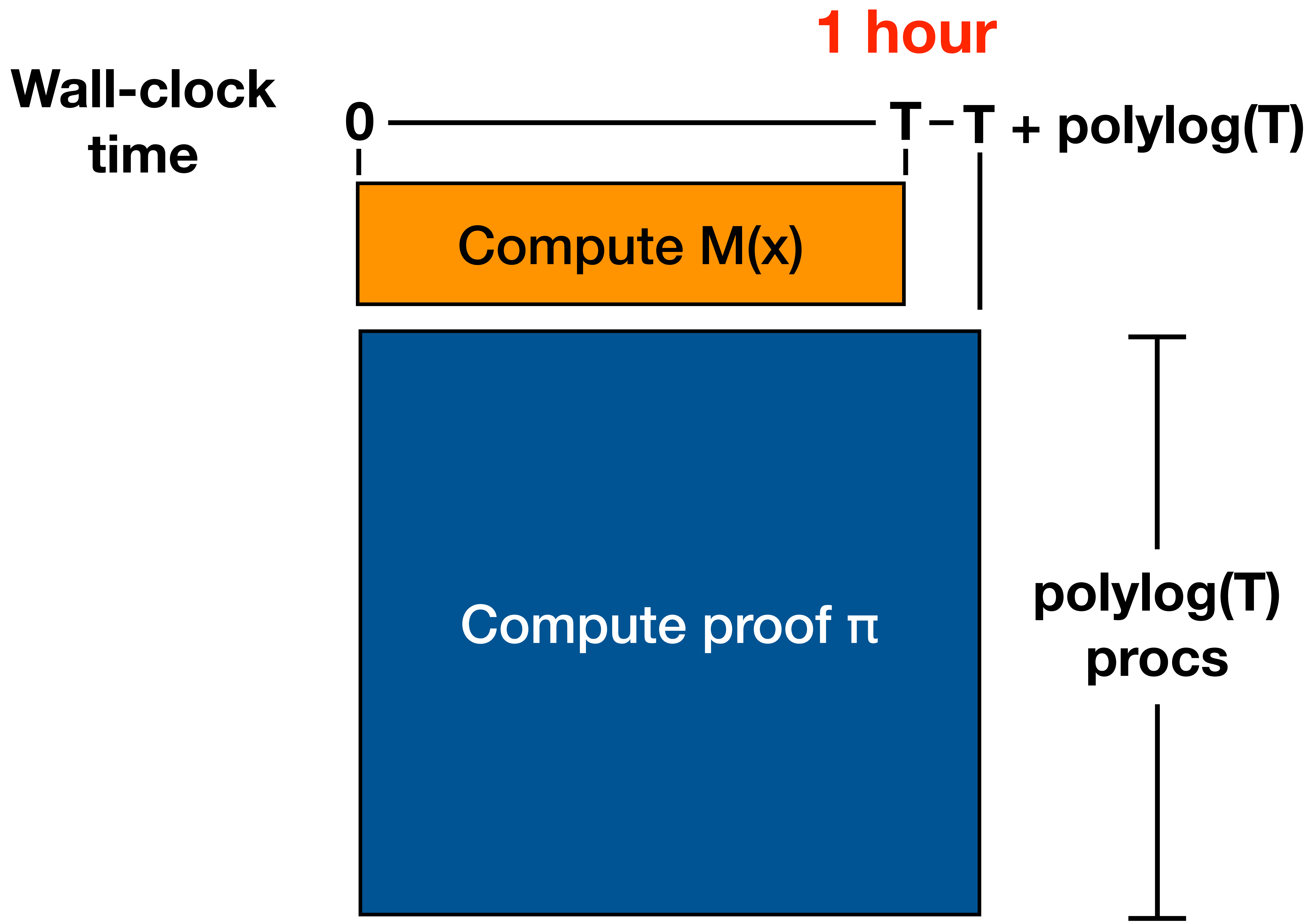

Compute the proof
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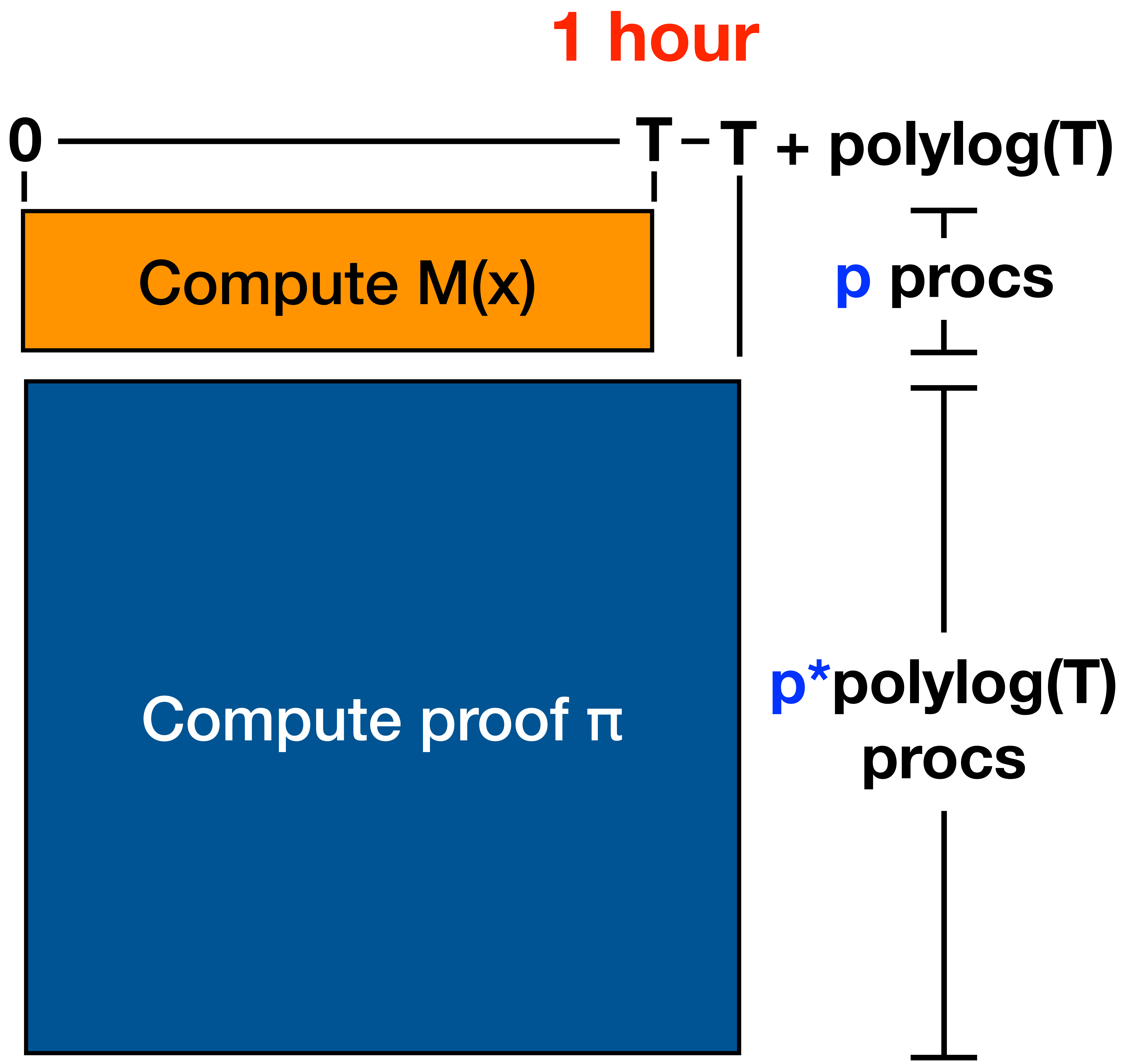
SPARG:
Parallelizable Delegation for PRAM

Wall-clock time



Compute the proof
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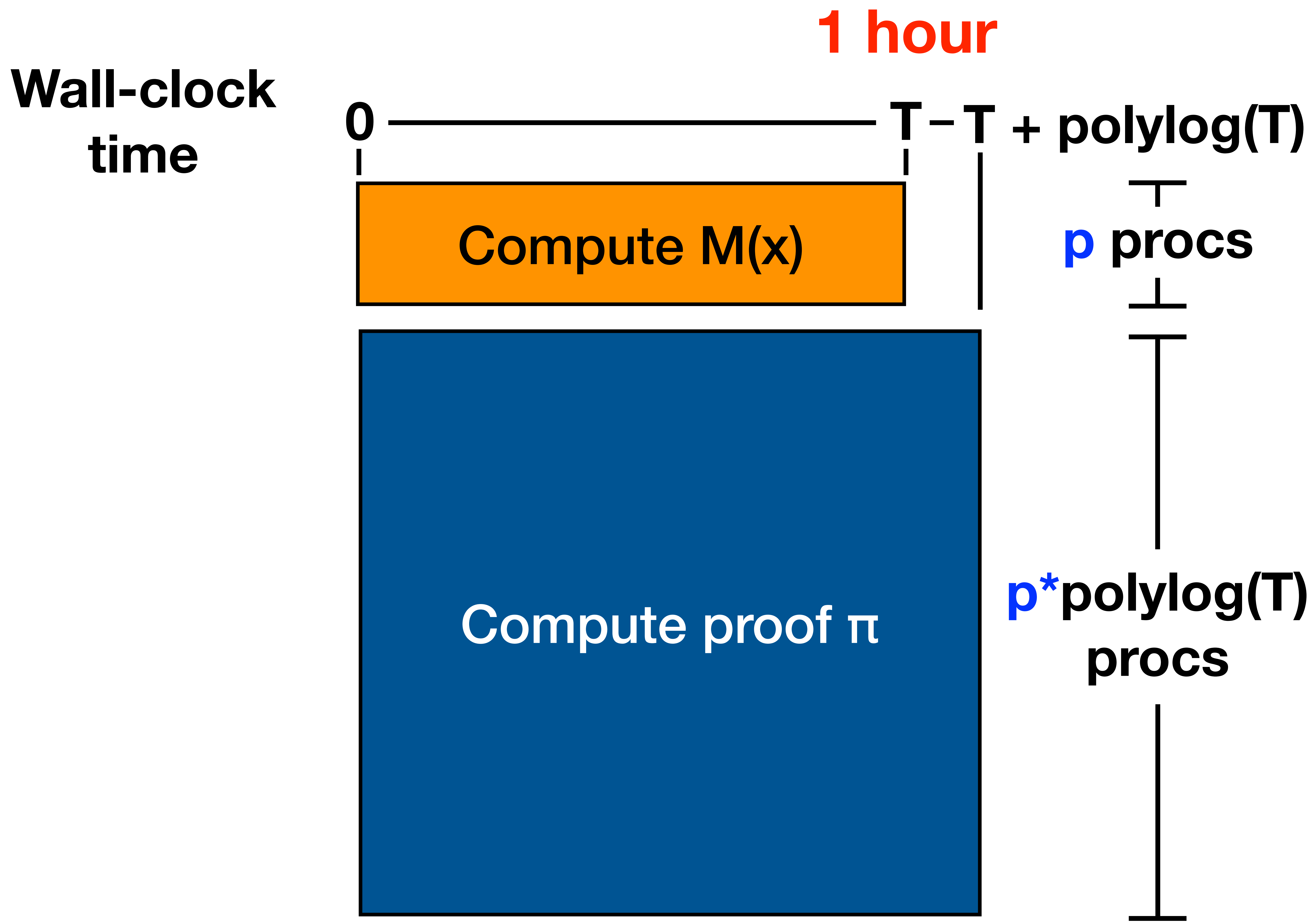
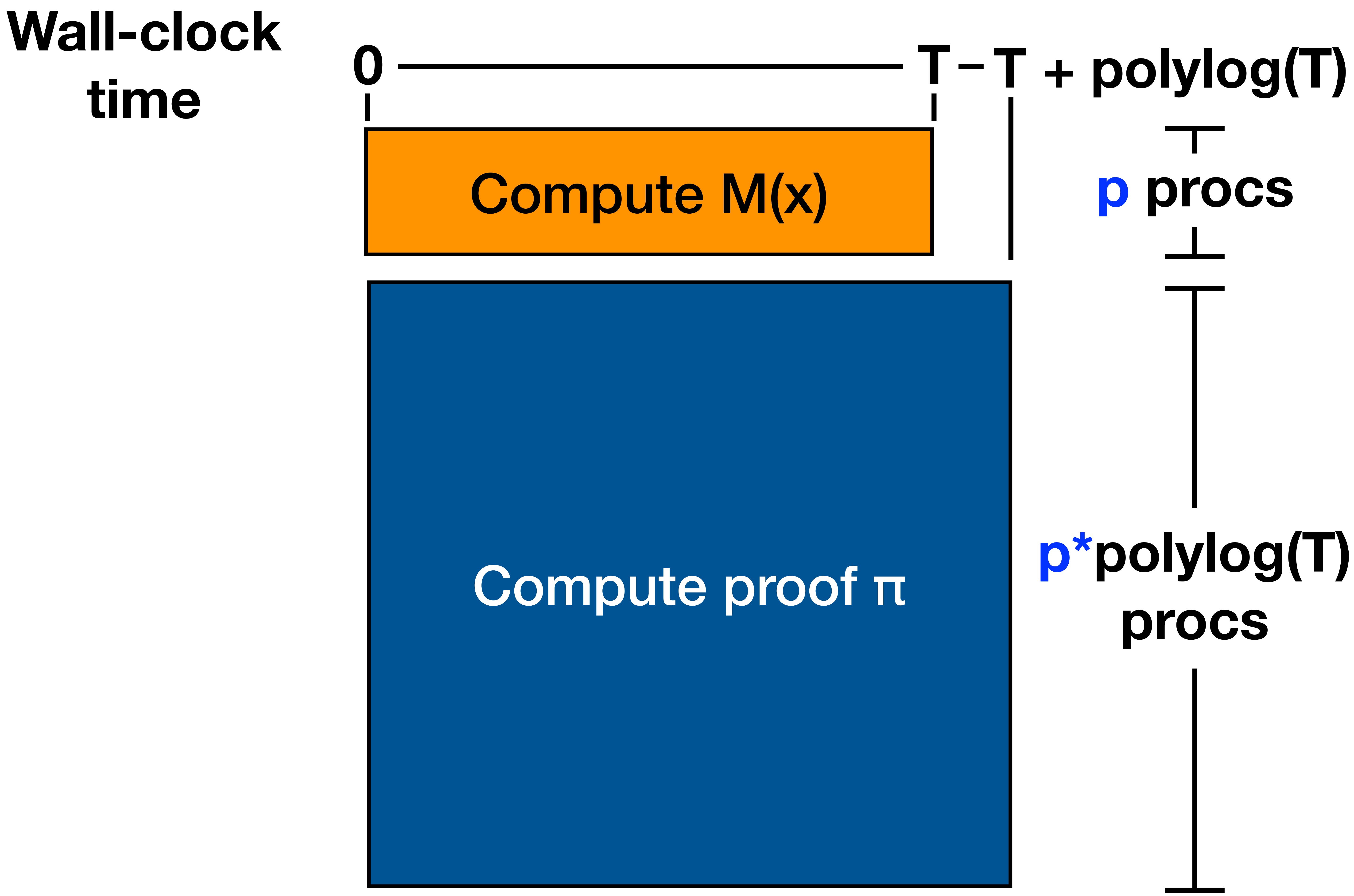


Compute the proof ***in parallel*** *to the computation*

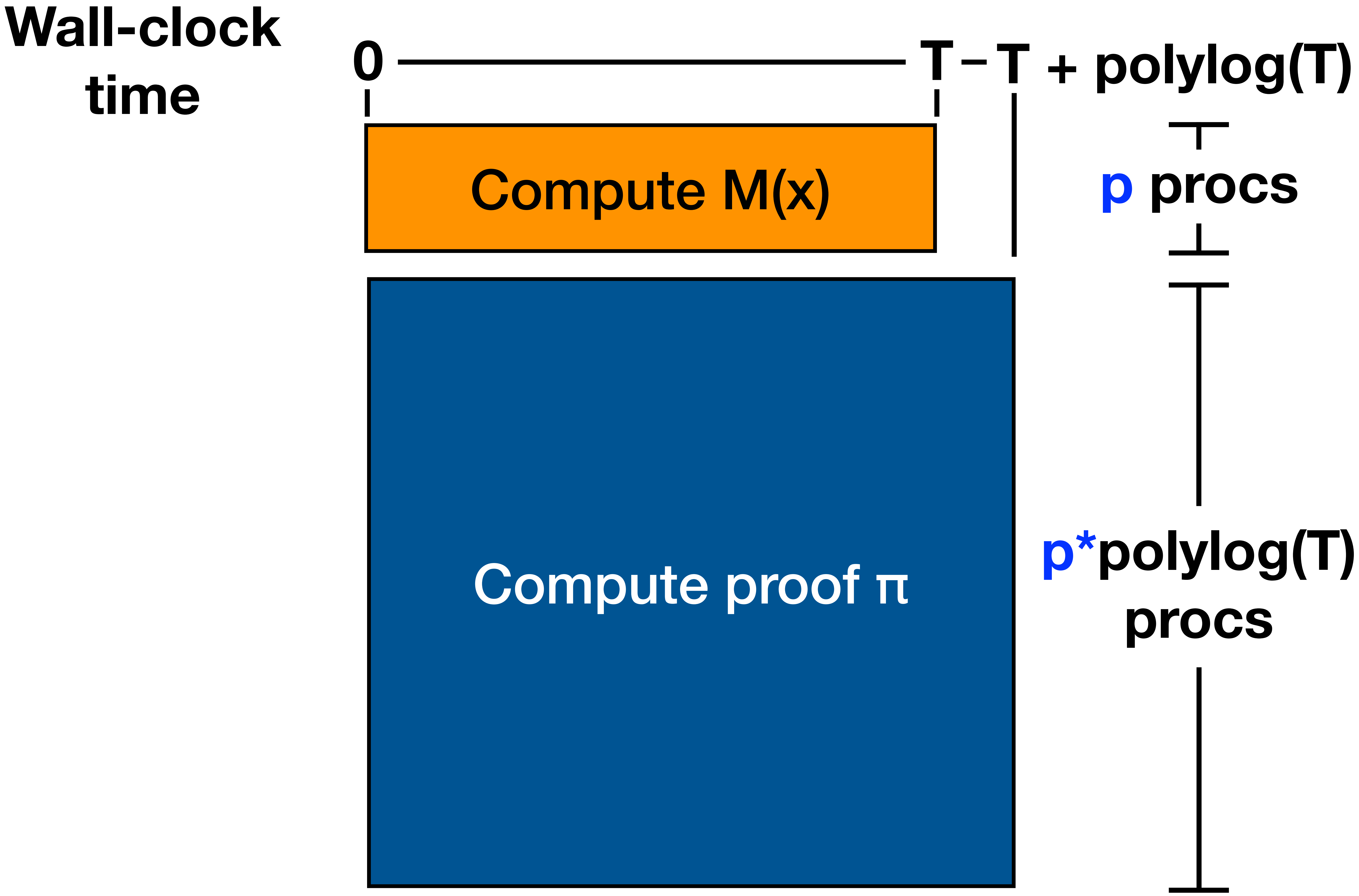
- Only known from **SNARKs** [EFKP20]

Main Result



Wall-clock time
0
T
T + polylog(T)
Compute M(x)
p procs
Compute proof π
p*polylog(T) procs

Main Result



Theorem:

Assuming **LWE**, there exists parallelizable delegation for *any* PRAM computation.

Application:
Verifiable Delay Functions [BBBF18]

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- Verifiable function that **cannot be sped up** with **many processors**

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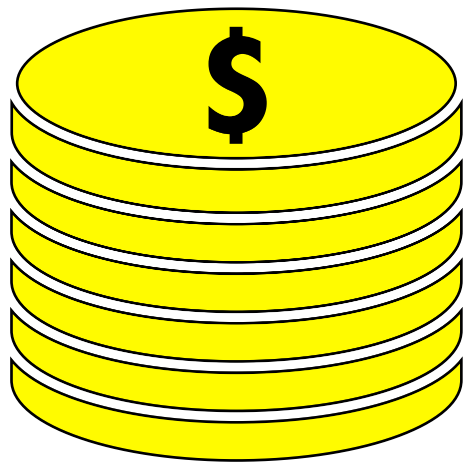

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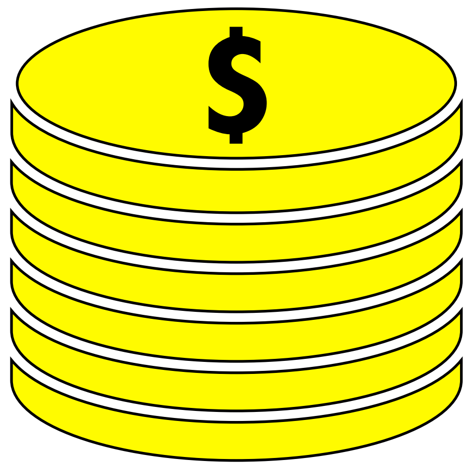
- Verifiable function that **cannot be sped up** with **many processors** 

Plain model constructions:

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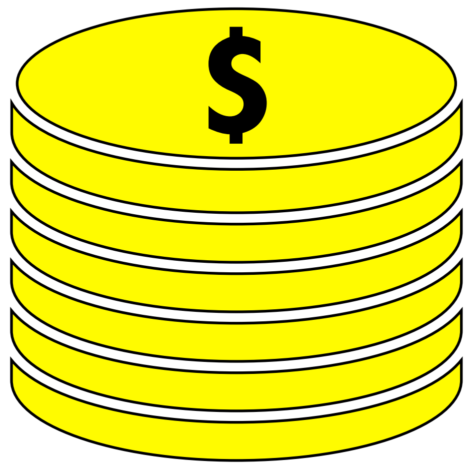

Plain model constructions:

Iterated Sequential Function
+ SNARGs for P
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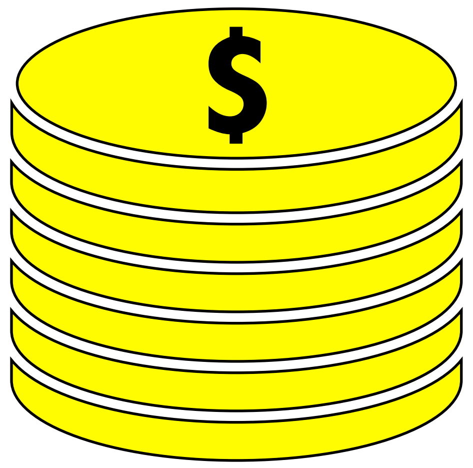

Plain model constructions:

Iterated Sequential Function + SNARGs for P [BBBF18]	*Any* Sequential Function + SNARKs for NP [EFKP20]

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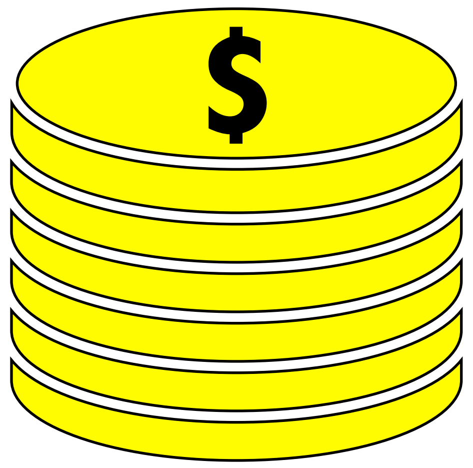
- Verifiable function that **cannot be sped up** with **many processors** 

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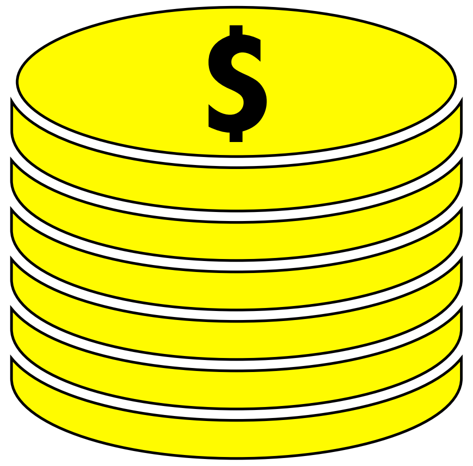

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SPARG Paradigm:

Any Function + SPARG => Verifiable Function

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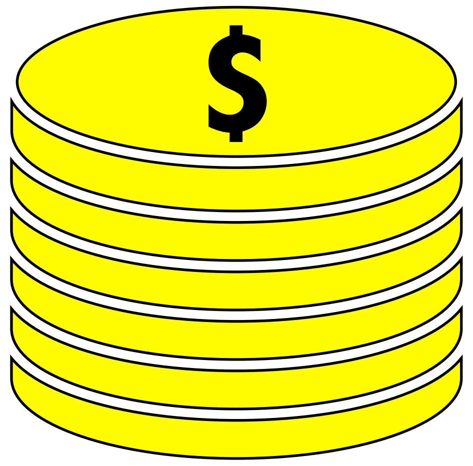

Plain model constructions:

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preserves parallel running time!

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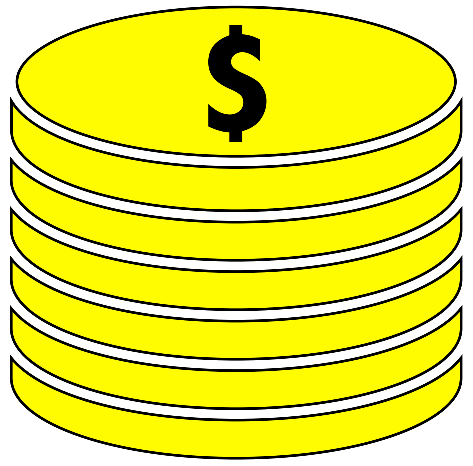

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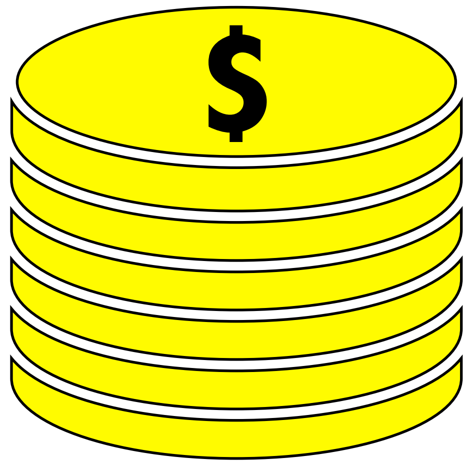

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Theorem:

Assuming **LWE** and *any* **sequential function**, there exists a VDF.

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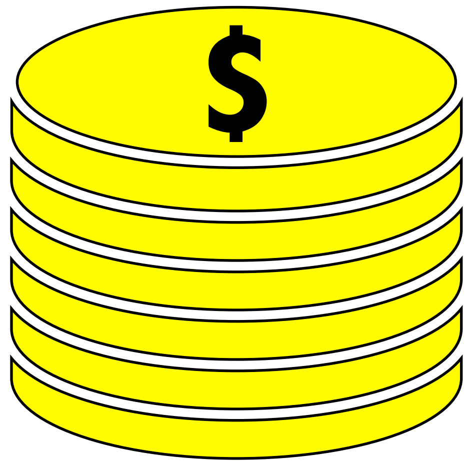

Plain model constructions:

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Minimal assumption

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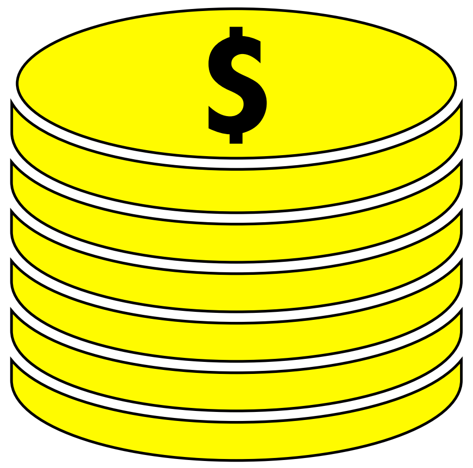
- Verifiable function that **cannot be sped up** with **many processors** 

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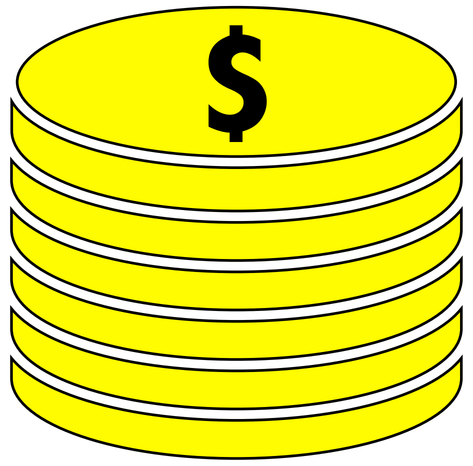

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Assuming **LWE** and *any* **sequential function**, there exists a VDF.

Theorem:

Assuming **LWE** and *any* **memory-hard sequential function**, there exists a **memory-hard** VDF.

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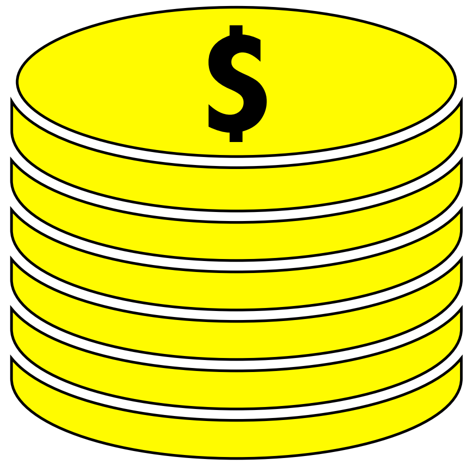

Plain model constructions:

Iterated Sequential Function + SNARGs for P [BBBF18]	***Any* Sequential Function + SNARKs for [EFKP20]**	**g 22]**

First construction without "knowledge" assumptions

Theorem:

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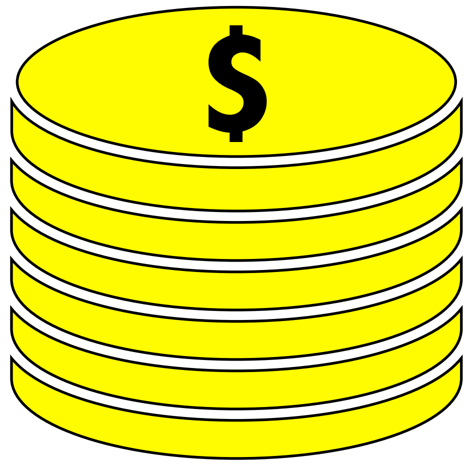

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Observation:
For standard arguments, can know the time bound **T** when you compute the proof.

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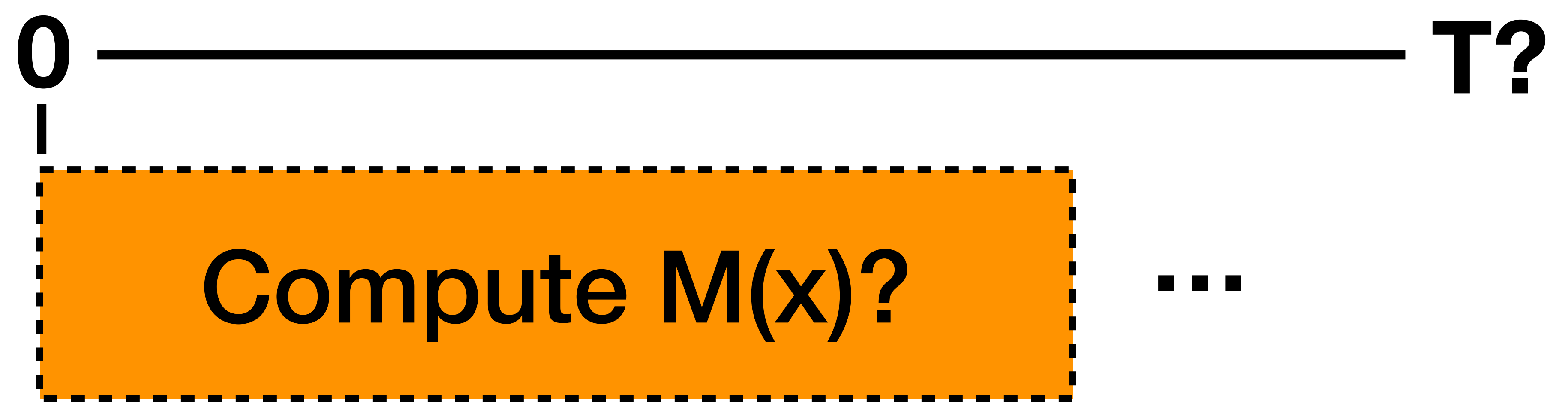
For SPARGs:



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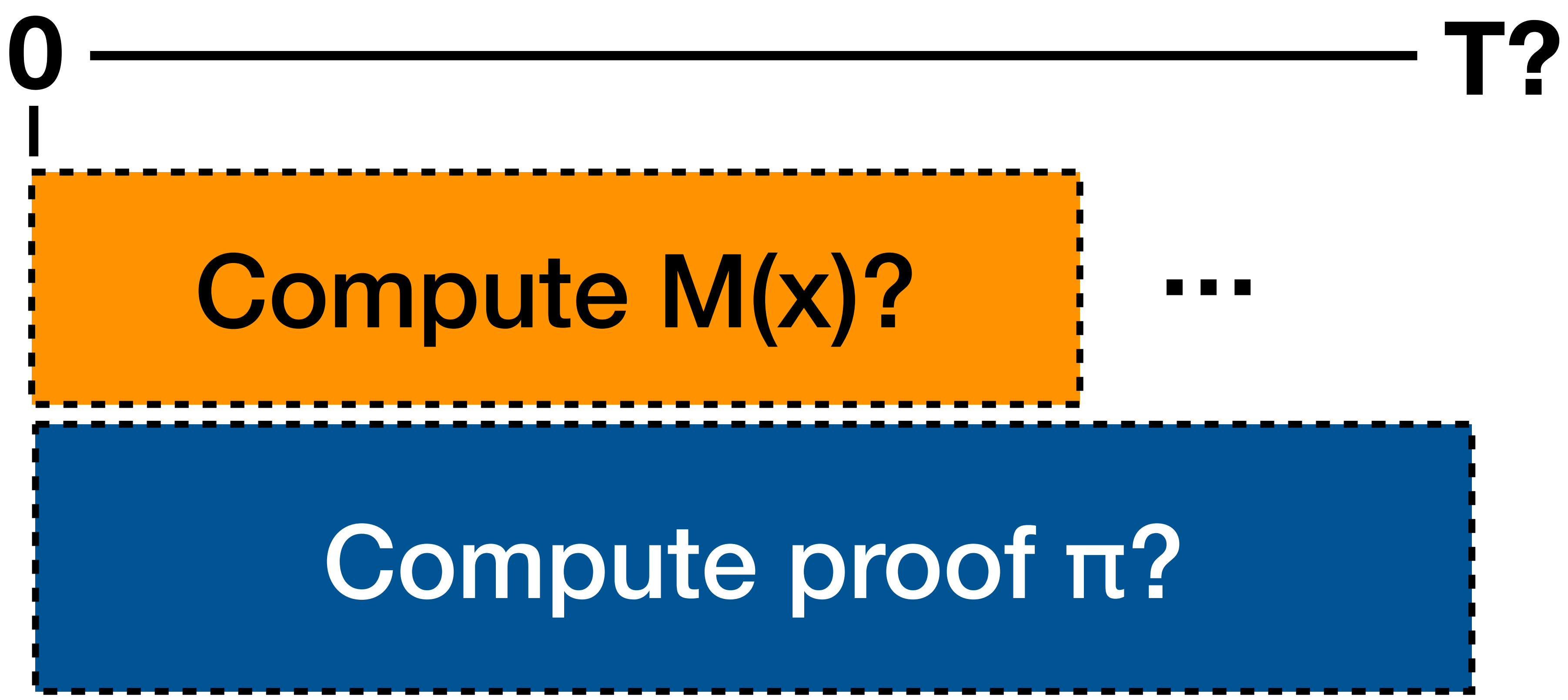

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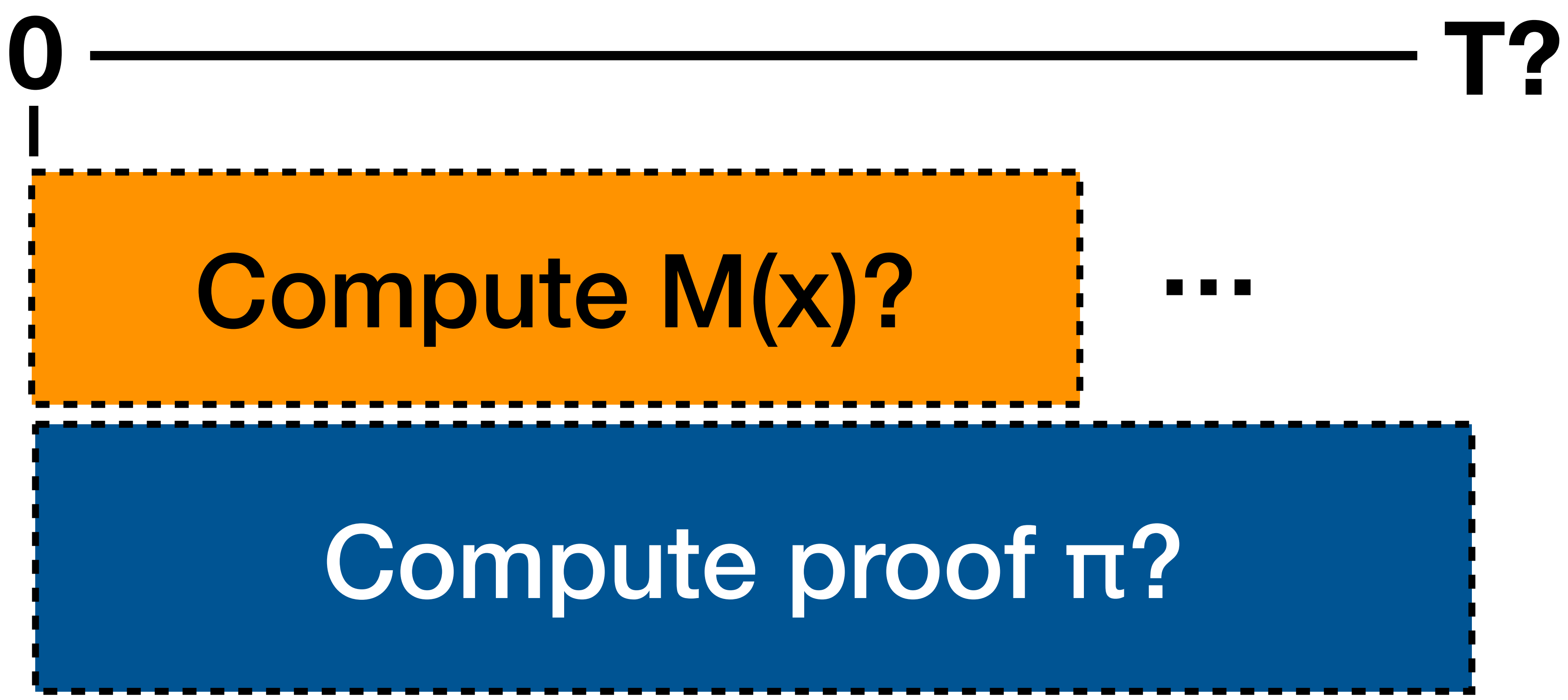

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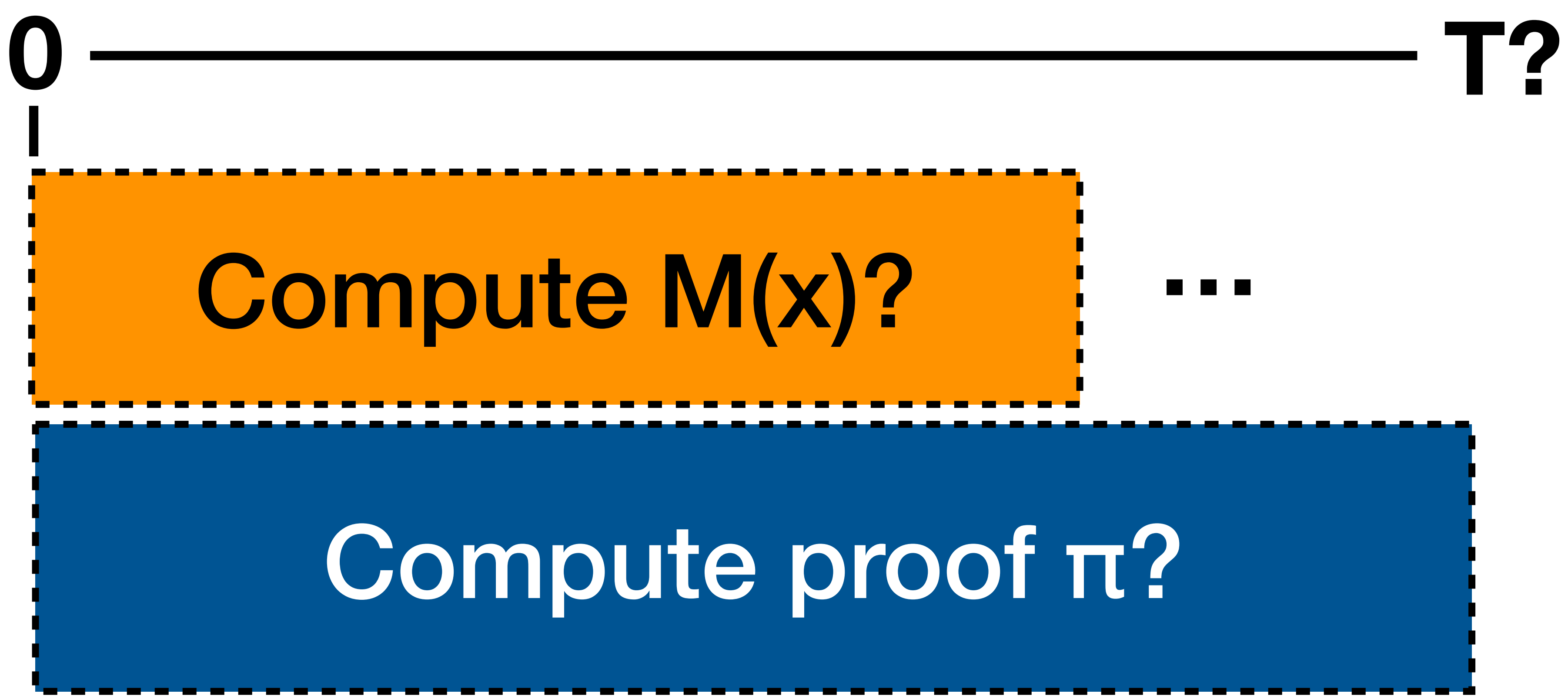

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Is this necessary?

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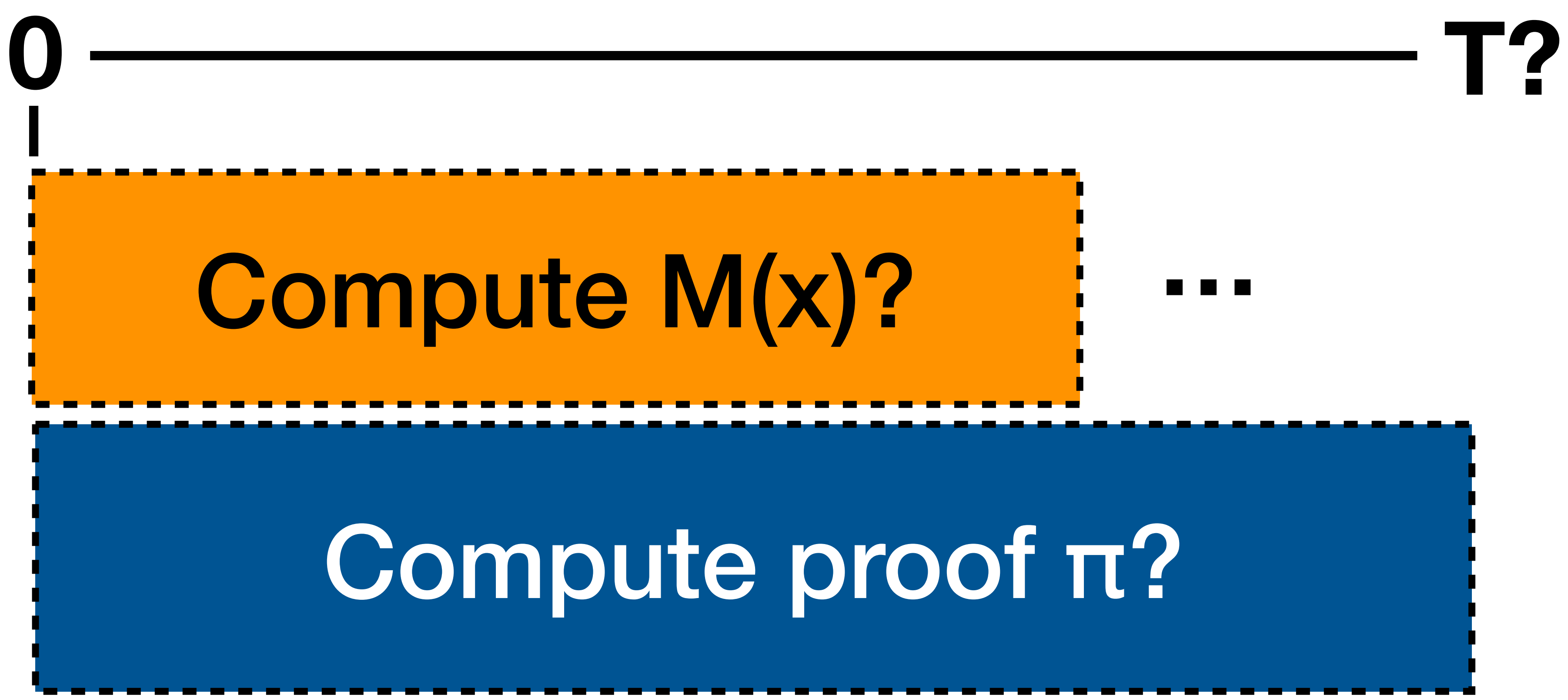

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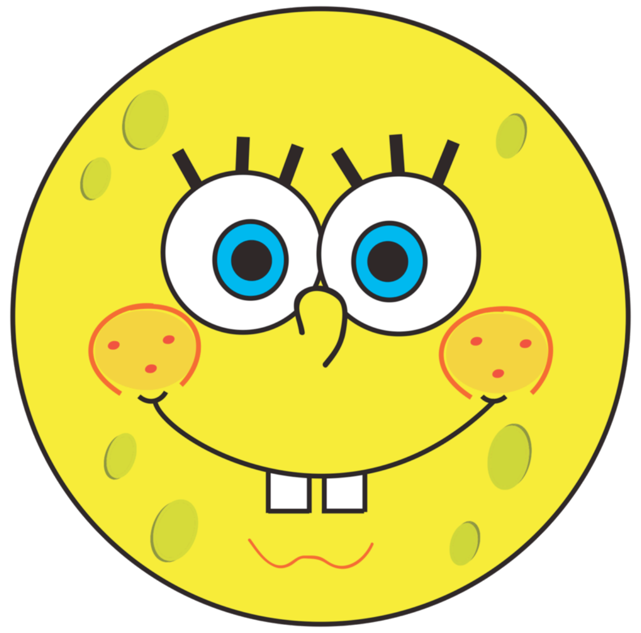
Is this necessary?

We show:
No!



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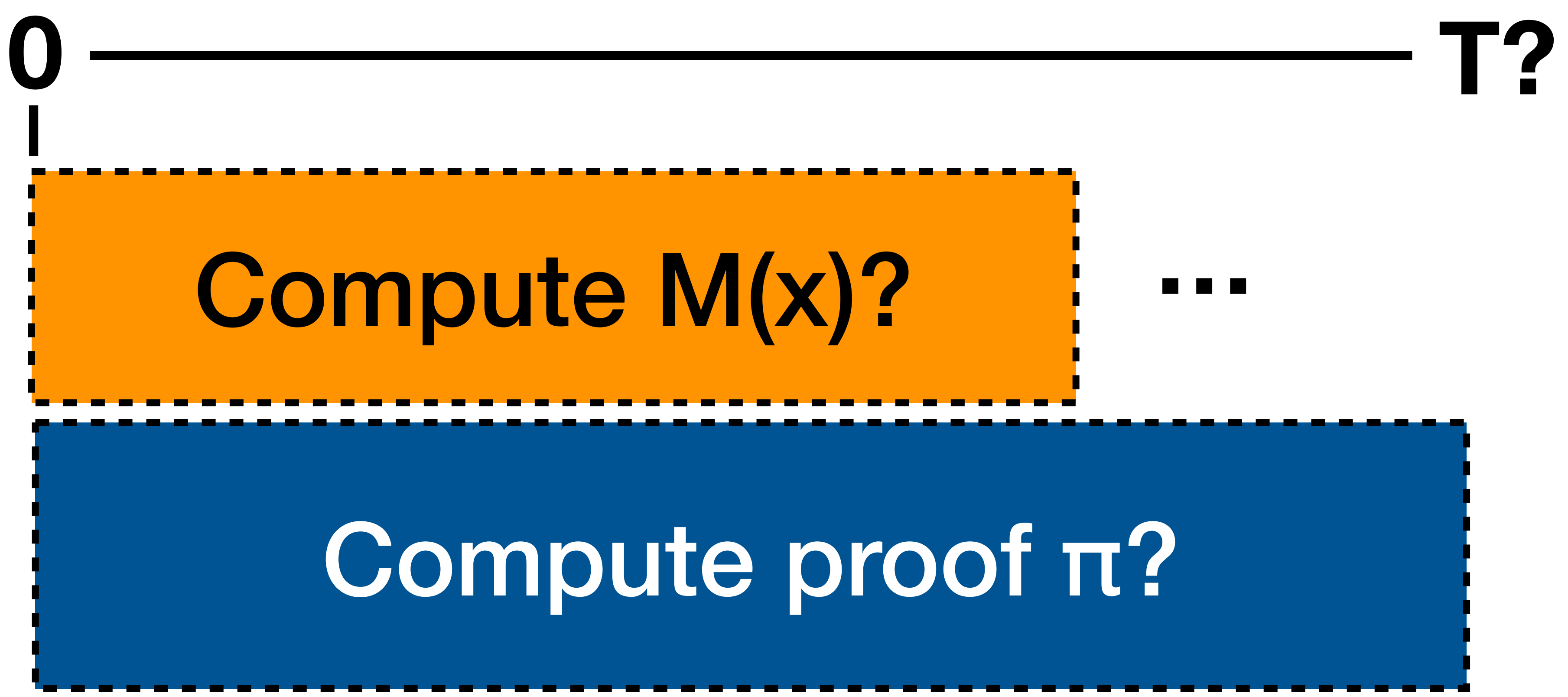

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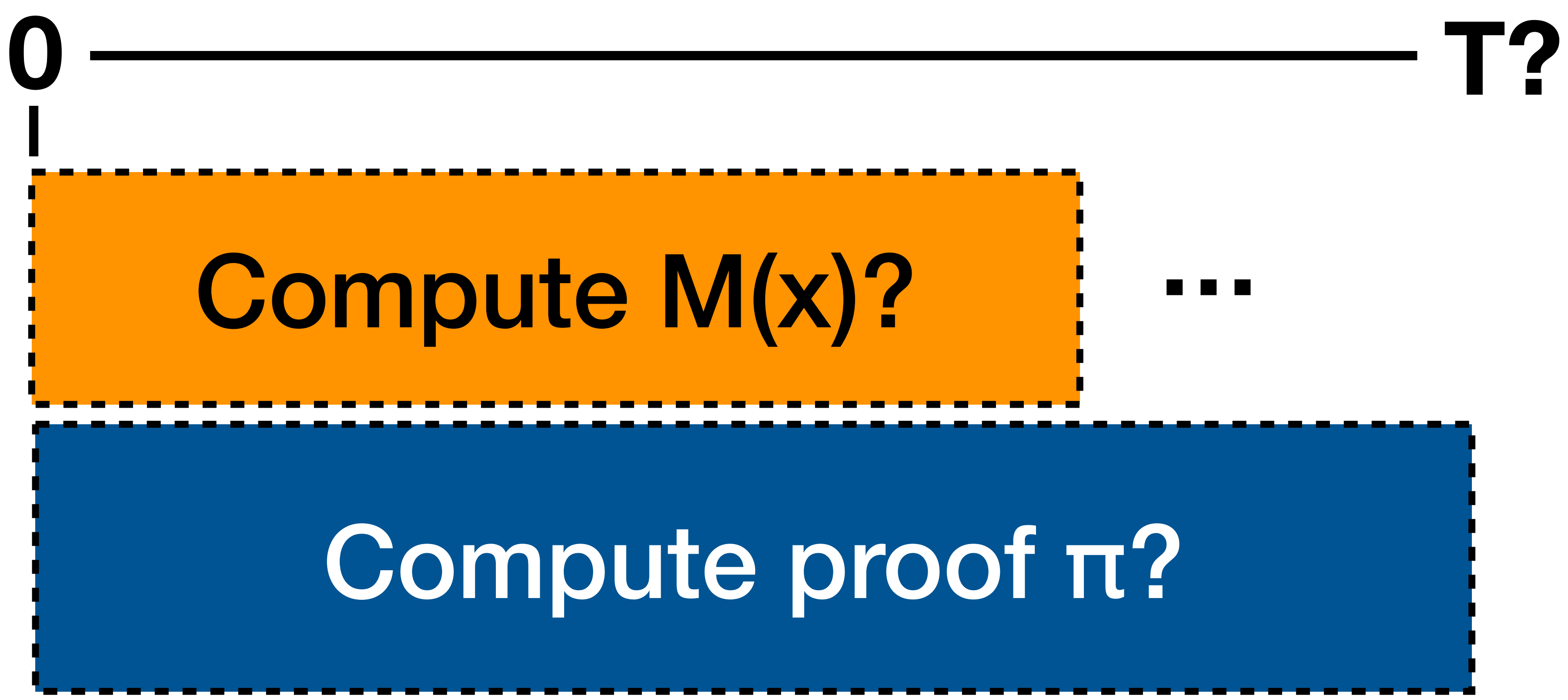

Theorem (informal):

Given *any* SPARG, can construct a **time-independent SPARG**.

Additional Result: Time-Independent SPARGs

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For standard arguments, can know the time bound **T** when you compute the proof.

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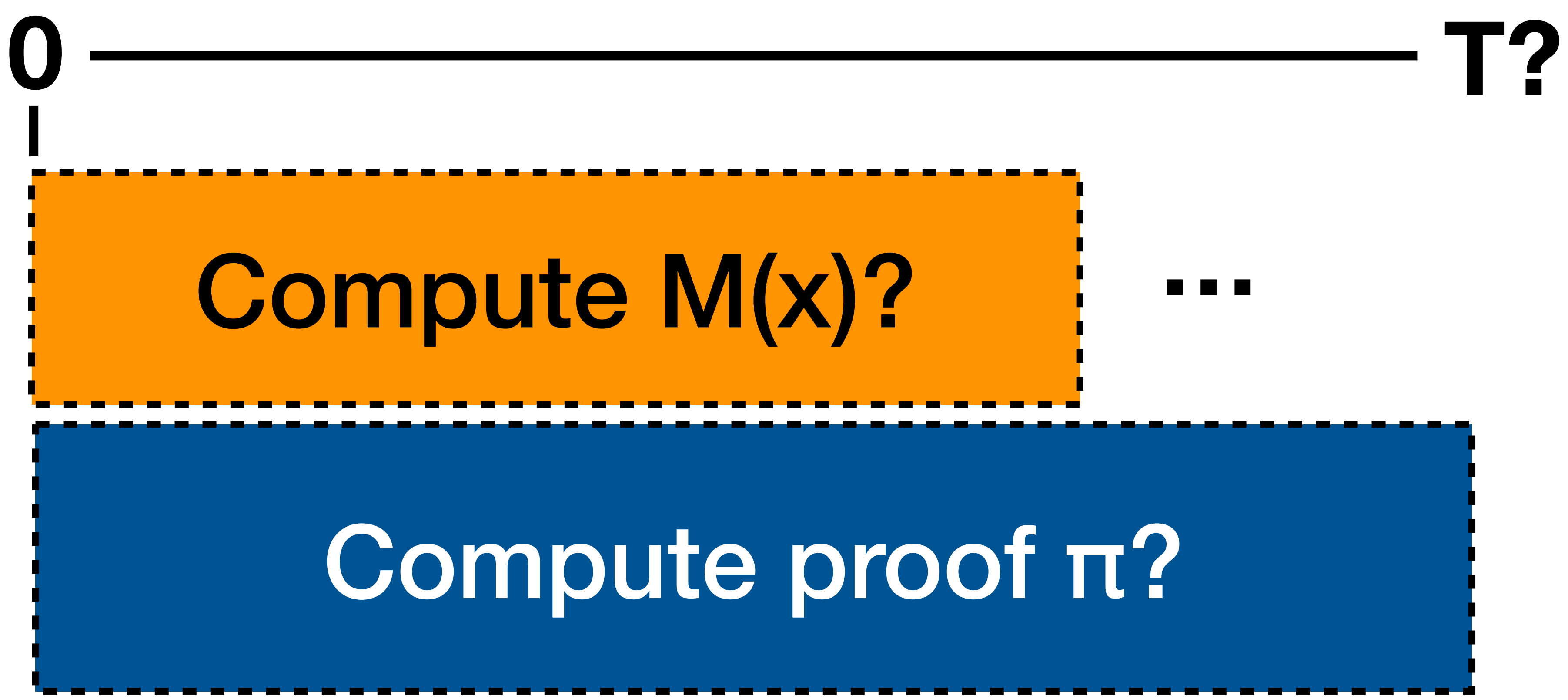

Theorem (informal):

Given *any* SPARG, can construct a **time-independent SPARG**.

Key idea:
Tree-based construction to "non-deterministically guess" binary representation of **T**.

Big Picture for
Our Main Result

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[EFKP20]

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Any SNARK for NP => [BCCT13] Quasi-linear SNARK for NP

Big Picture for Our Main Result

[EFKP20]

Any SNARK for NP **=>** [BCCT13] **Quasi-linear SNARK for NP** $\xrightarrow{\text{generic transformation}}$ **SPARKs for NP**

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Our Work

Big Picture for Our Main Result

[EFKP20]

Any SNARK for NP $\underset{\text{[BCCT13]}}{=>}$ Quasi-linear SNARK for NP $\xrightarrow{\text{generic transformation}}$ SPARKs for NP

Our Work

Specific SNARG for P from LWE [CJJ21] => **Quasi-linear updatable RAM delegation**

Big Picture for Our Main Result

[EFKP20]

Any SNARK for NP => [BCCT13] Quasi-linear SNARK for NP $\xrightarrow{\text{generic transformation}}$ **SPARKs for NP**

Our Work

Specific SNARG for P from LWE [CJJ21] => **Quasi-linear updatable RAM delegation** $\xrightarrow{\text{generic transformation}}$ **SPARGs for P**

Quasi-linear Updatable RAM Delegation

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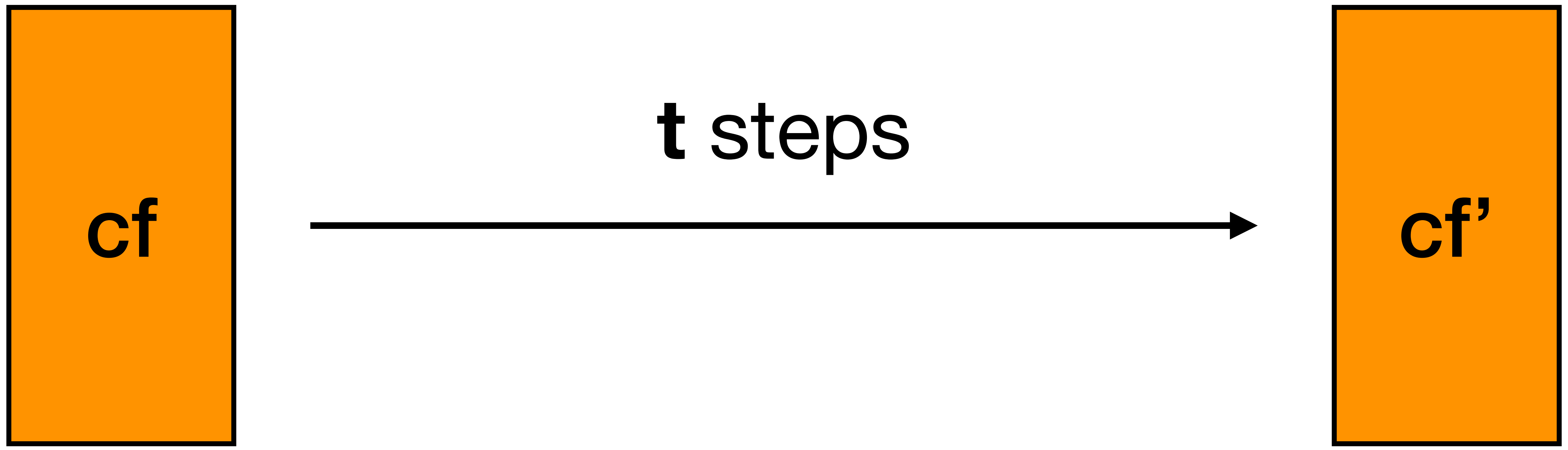
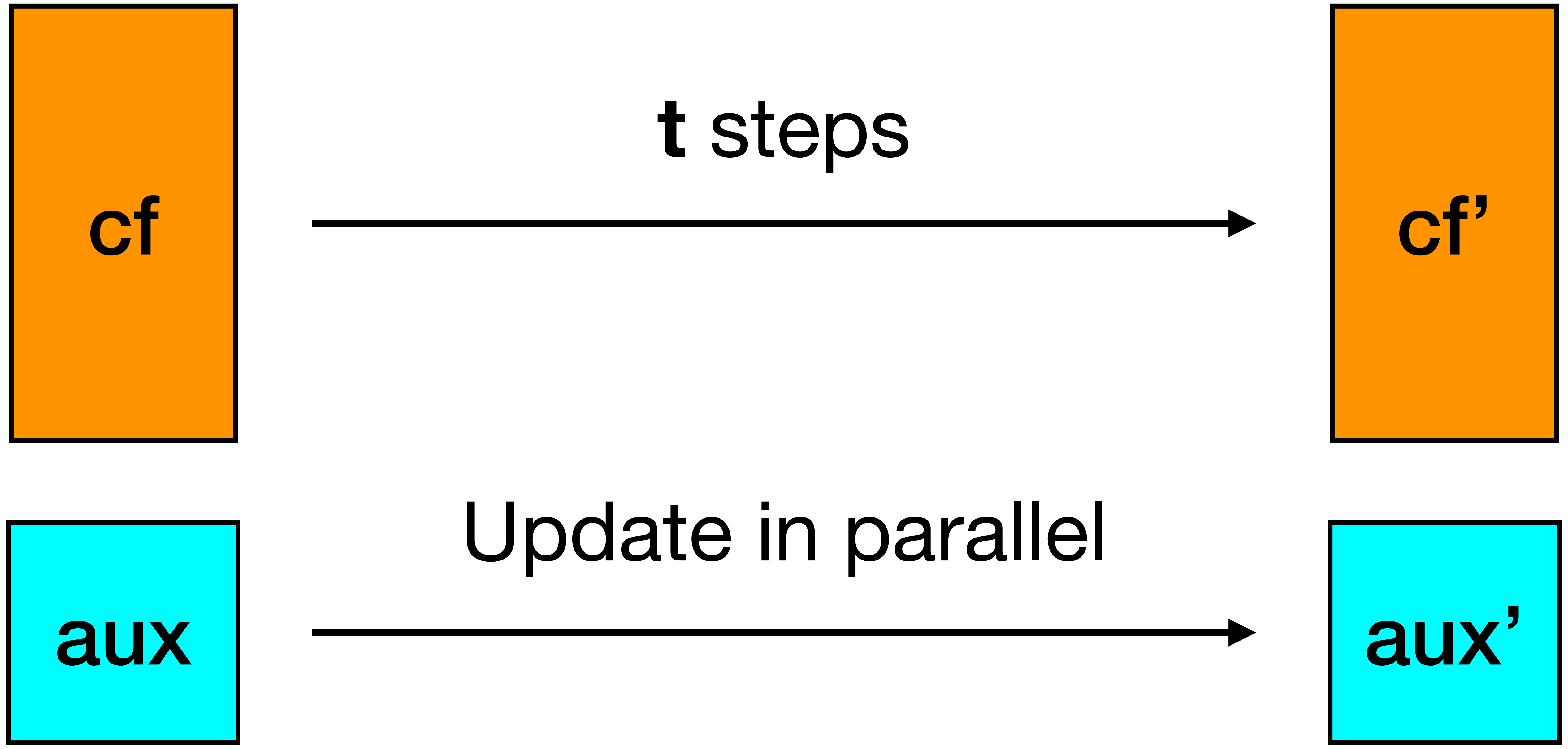
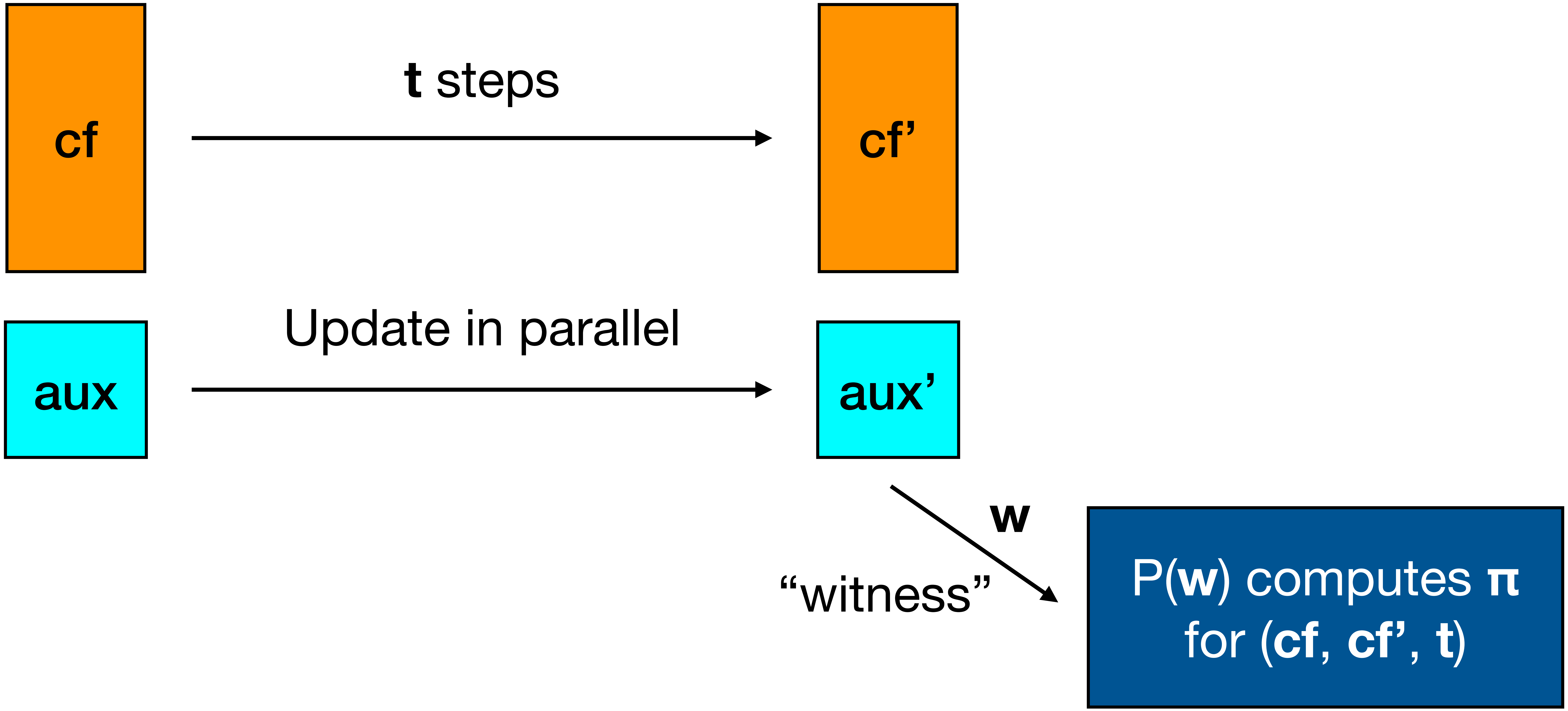


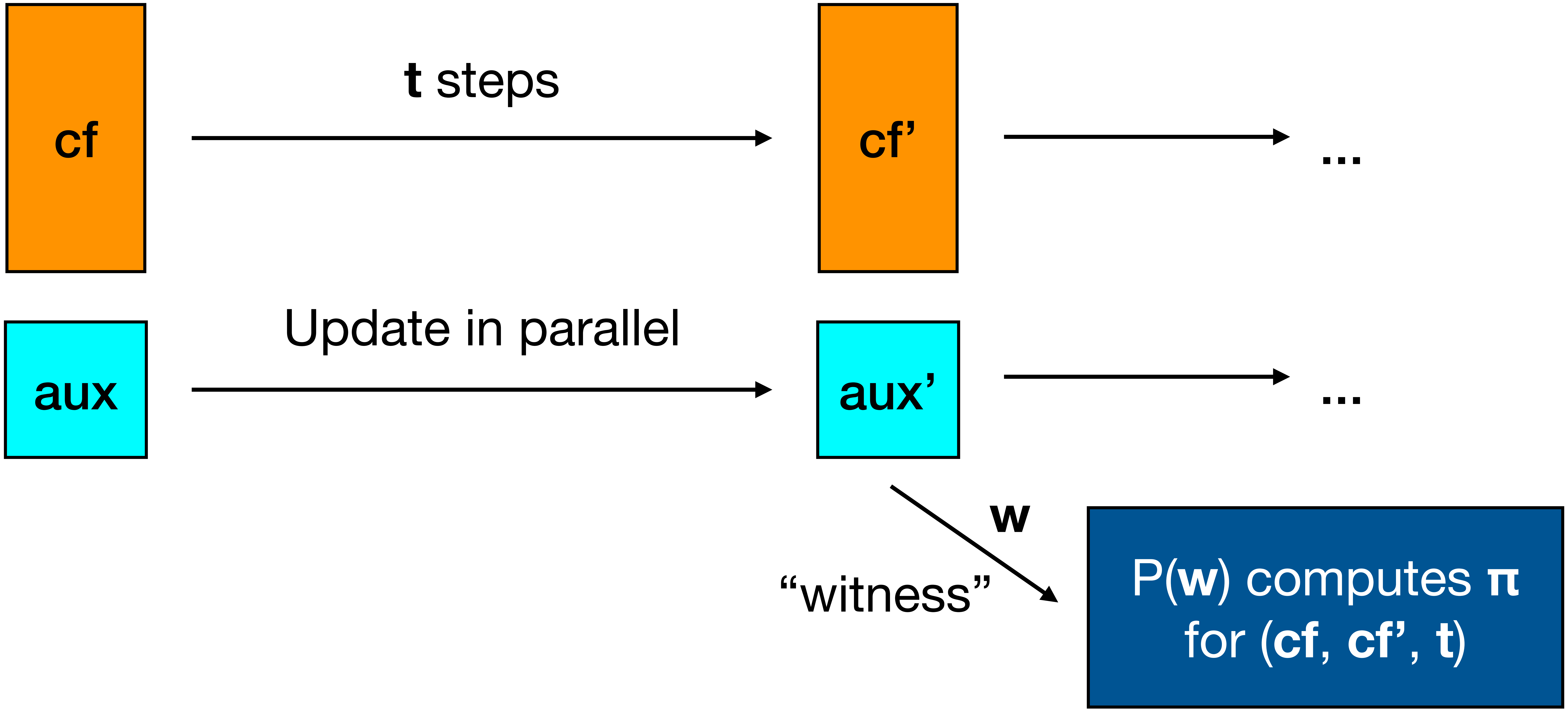
Quasi-linear Updatable RAM Delegation



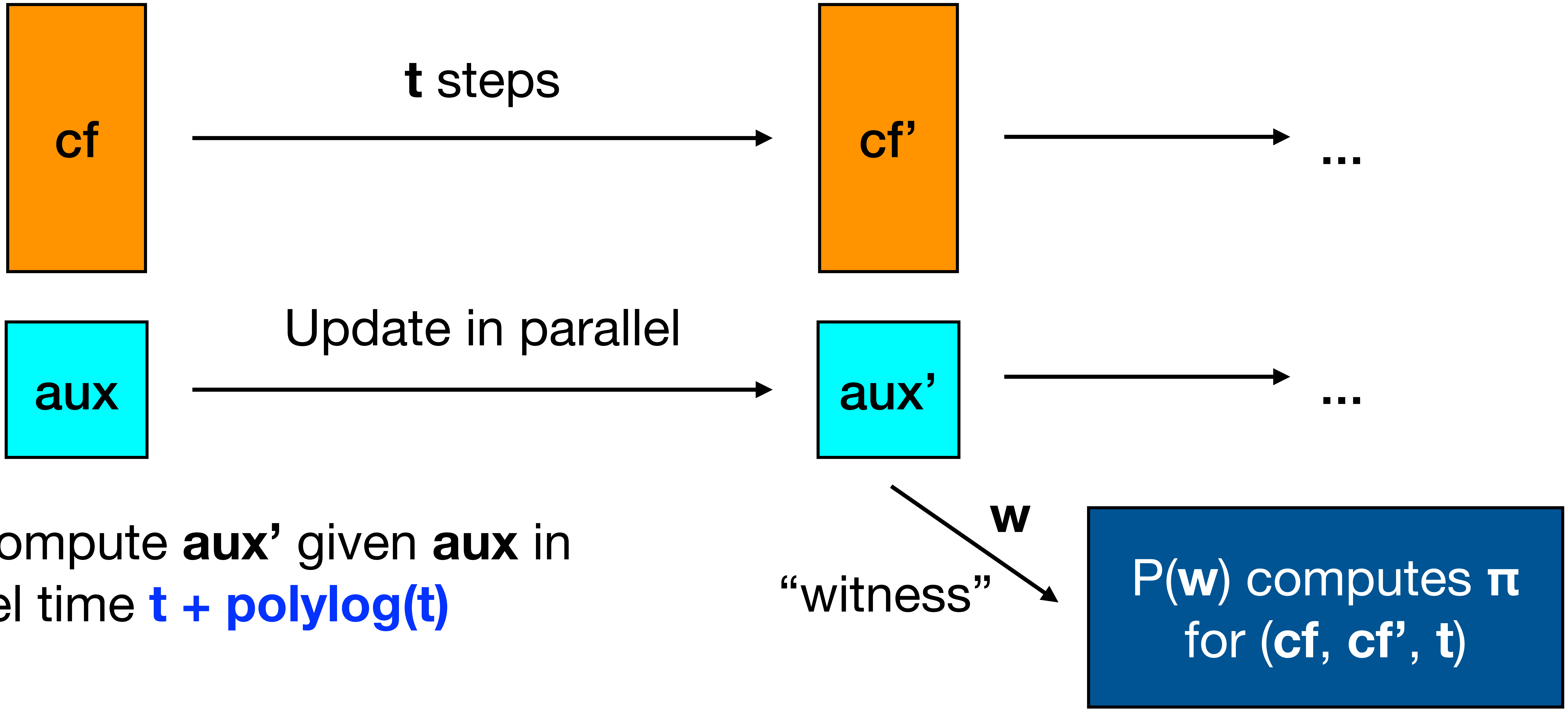
Quasi-linear Updatable RAM Delegation



Quasi-linear Updatable RAM Delegation

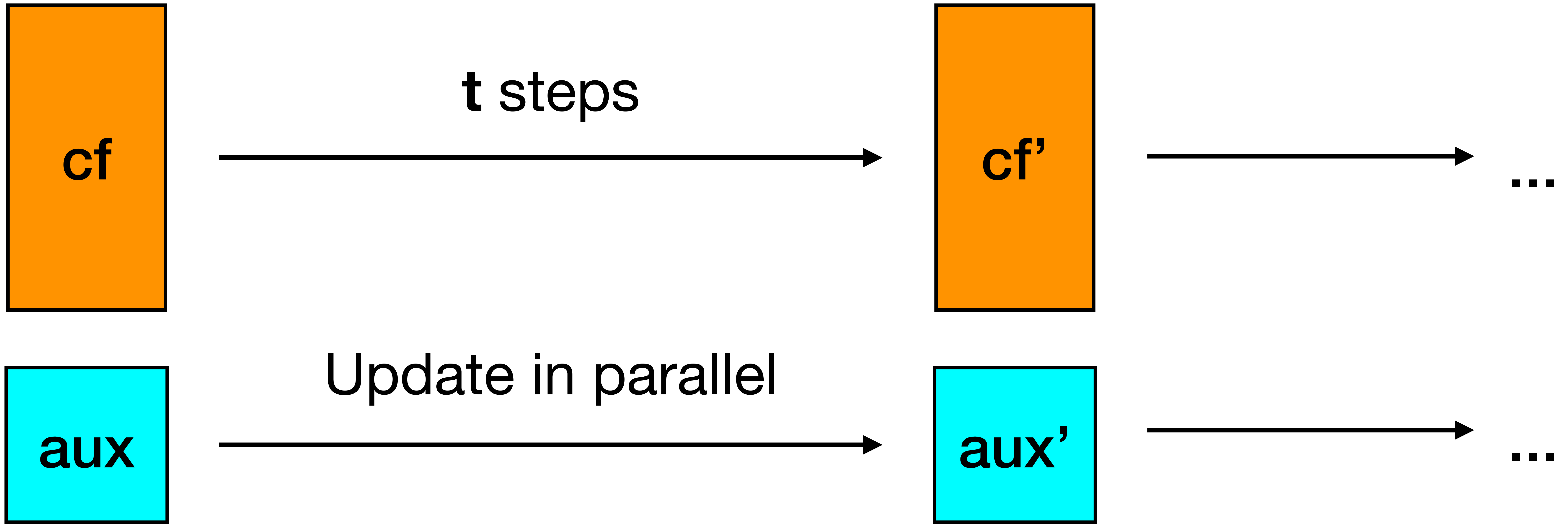


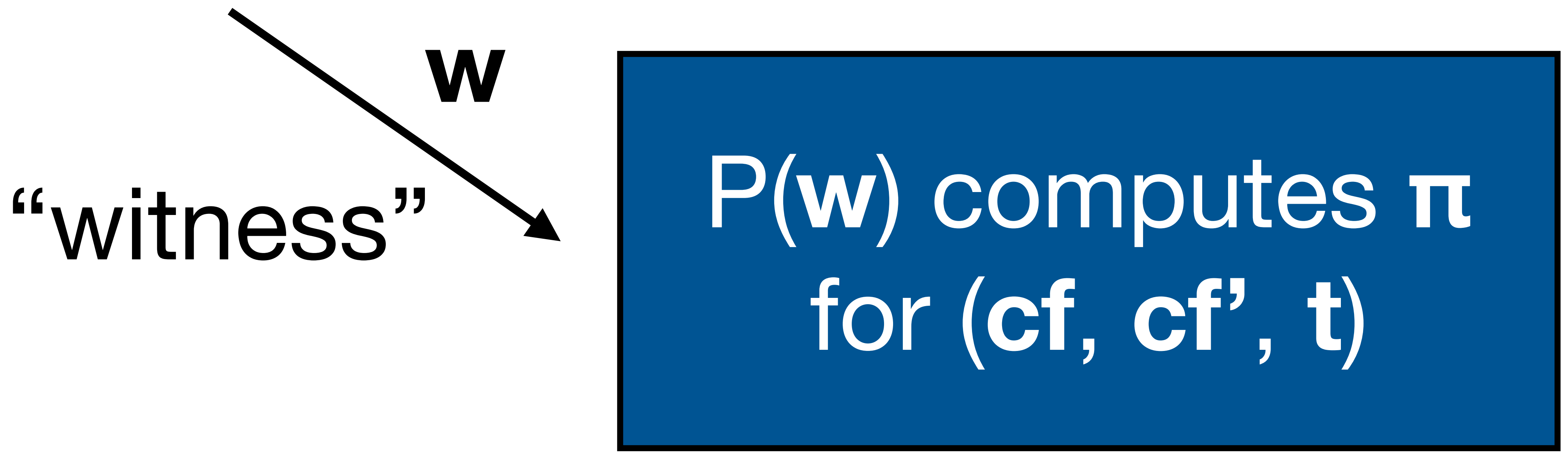
Quasi-linear Updatable RAM Delegation



- Can compute **aux’** given **aux** in parallel time **t + polylog(t)**

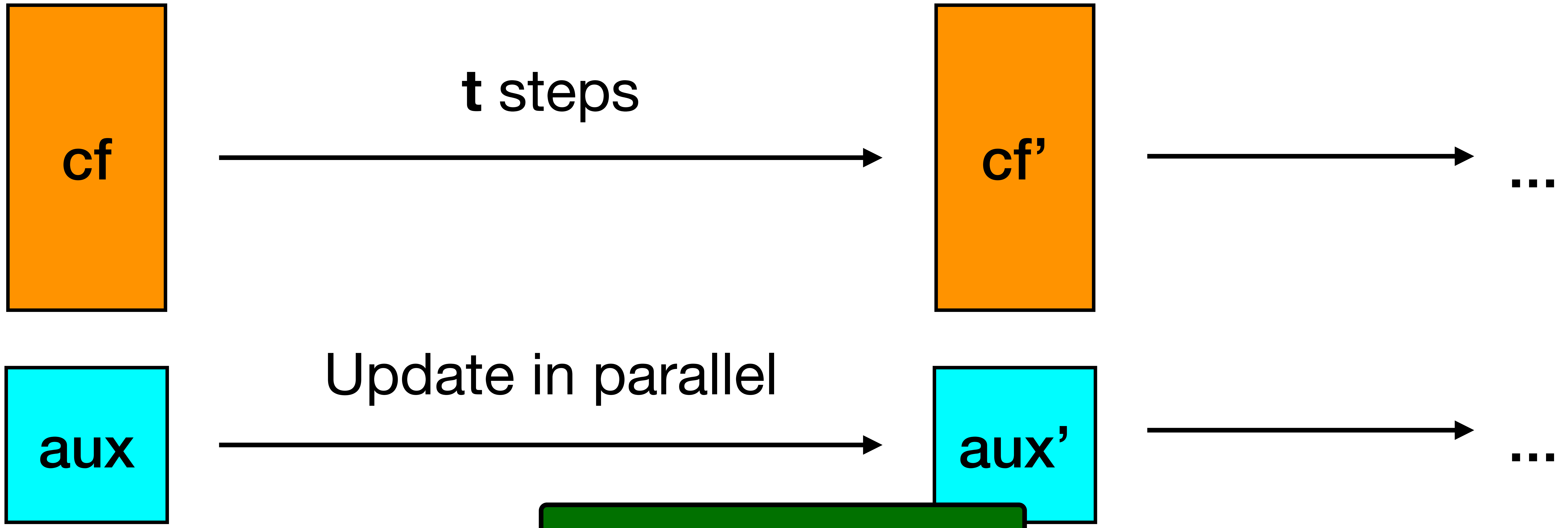
Quasi-linear Updatable RAM Delegation





- Can compute **aux’** given **aux** in parallel time **t + polylog(t)**
- Given **w**, can compute a proof **π** for **cf->cf’** in time **t *polylog(t)**

Quasi-linear Updatable RAM Delegation



- Can compute **aux’** given **au** parallel time **t + polylog(t)**
- Given **w**, can compute a proof **π** for **cf->cf’** in time **t *polylog(t)**

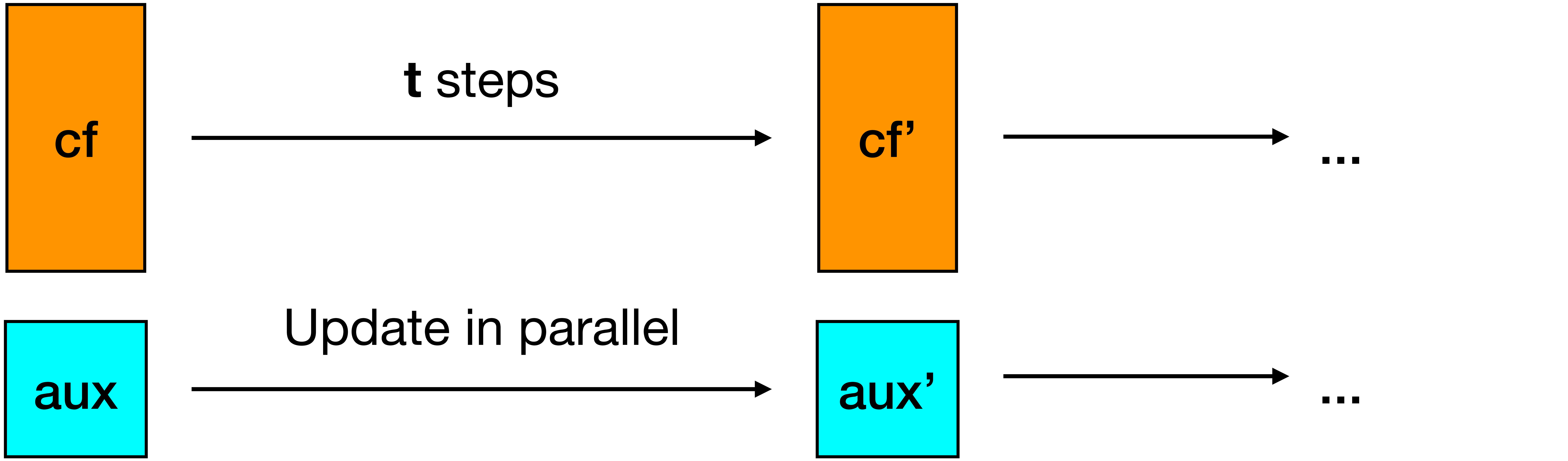
Without w, depends on |cf|.

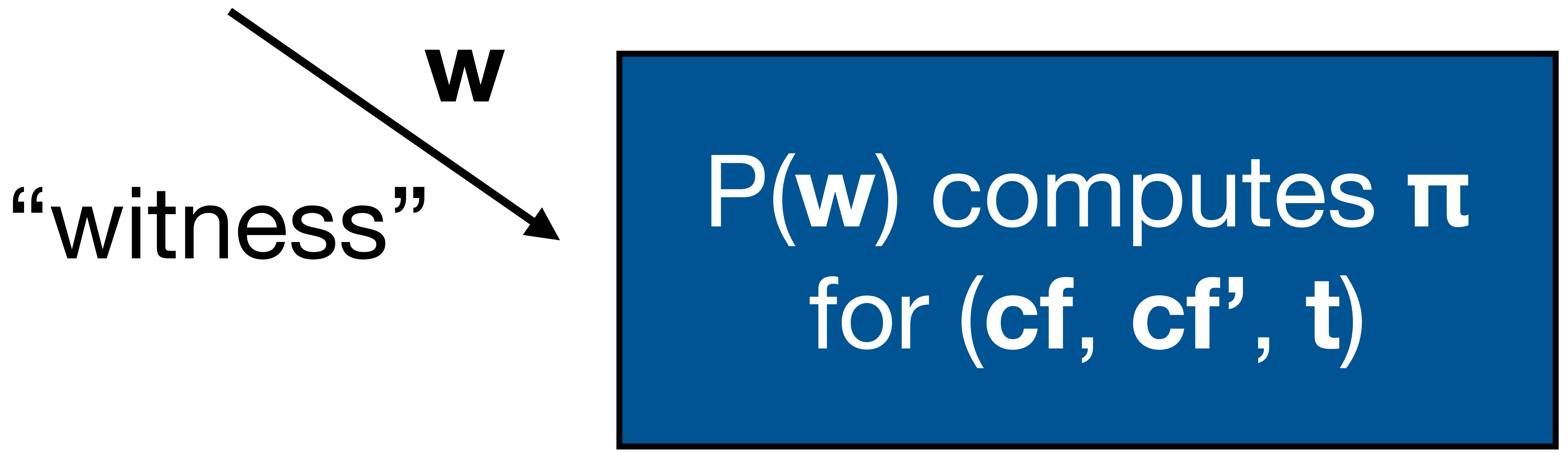
w

ess”

P(**w**) computes **π** for (**cf**, **cf’**, **t**)

Instantiating from LWE





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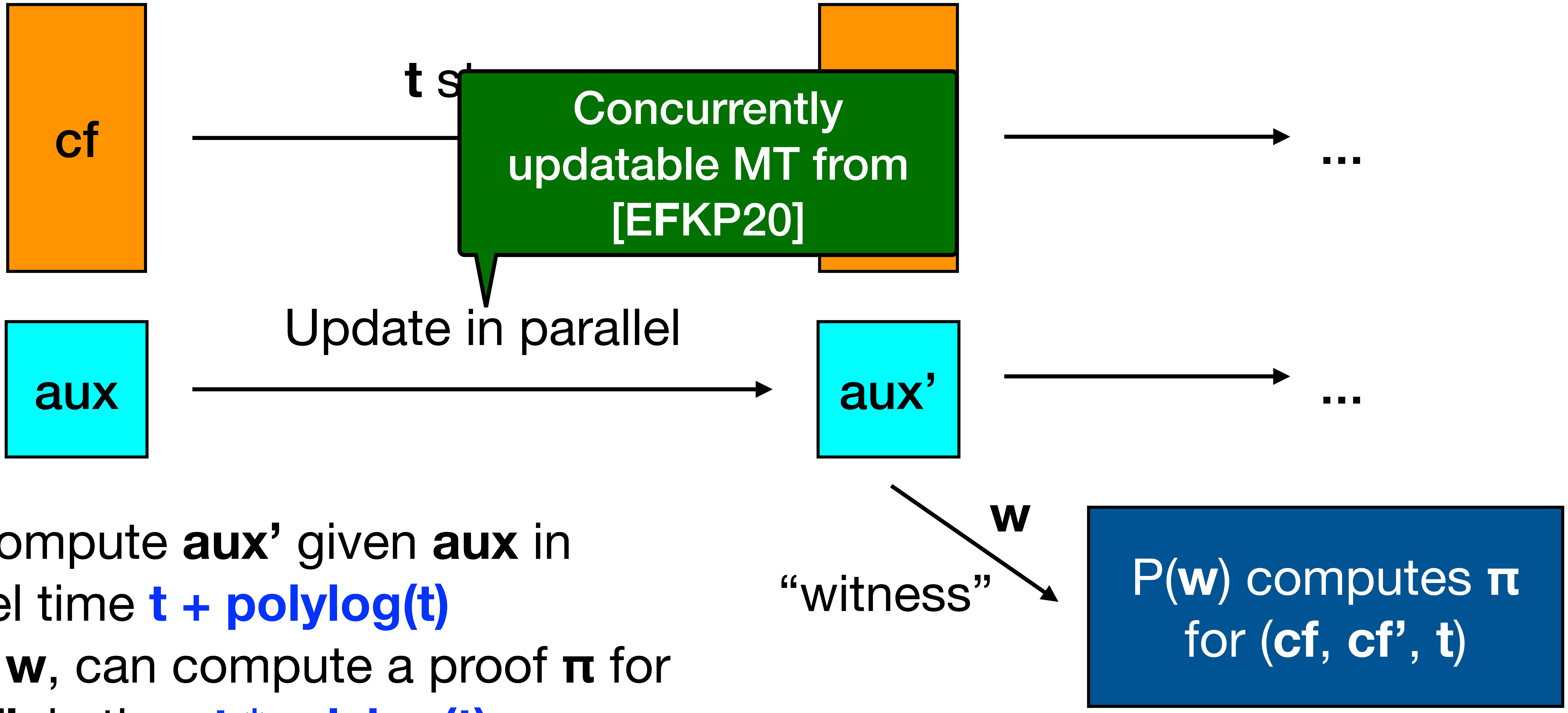

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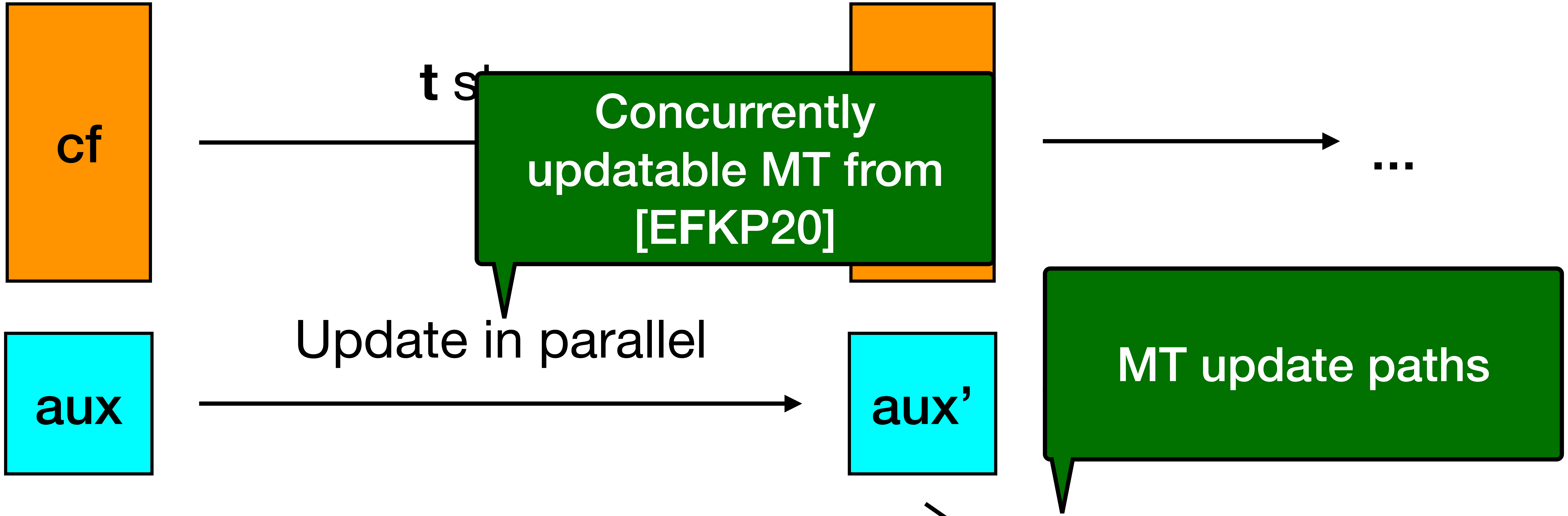

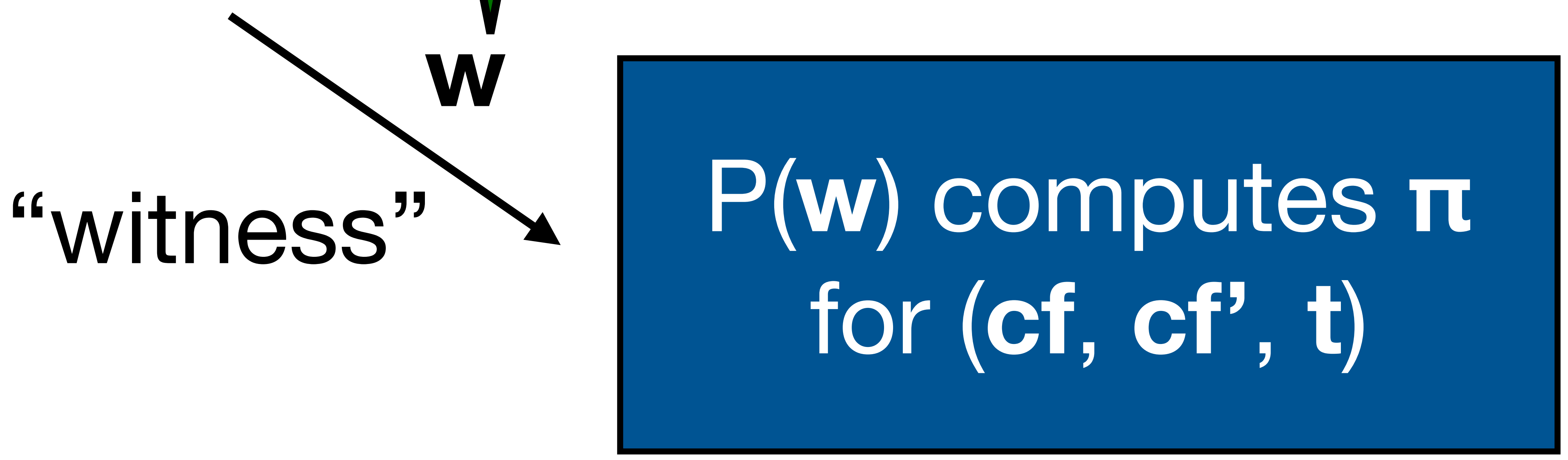

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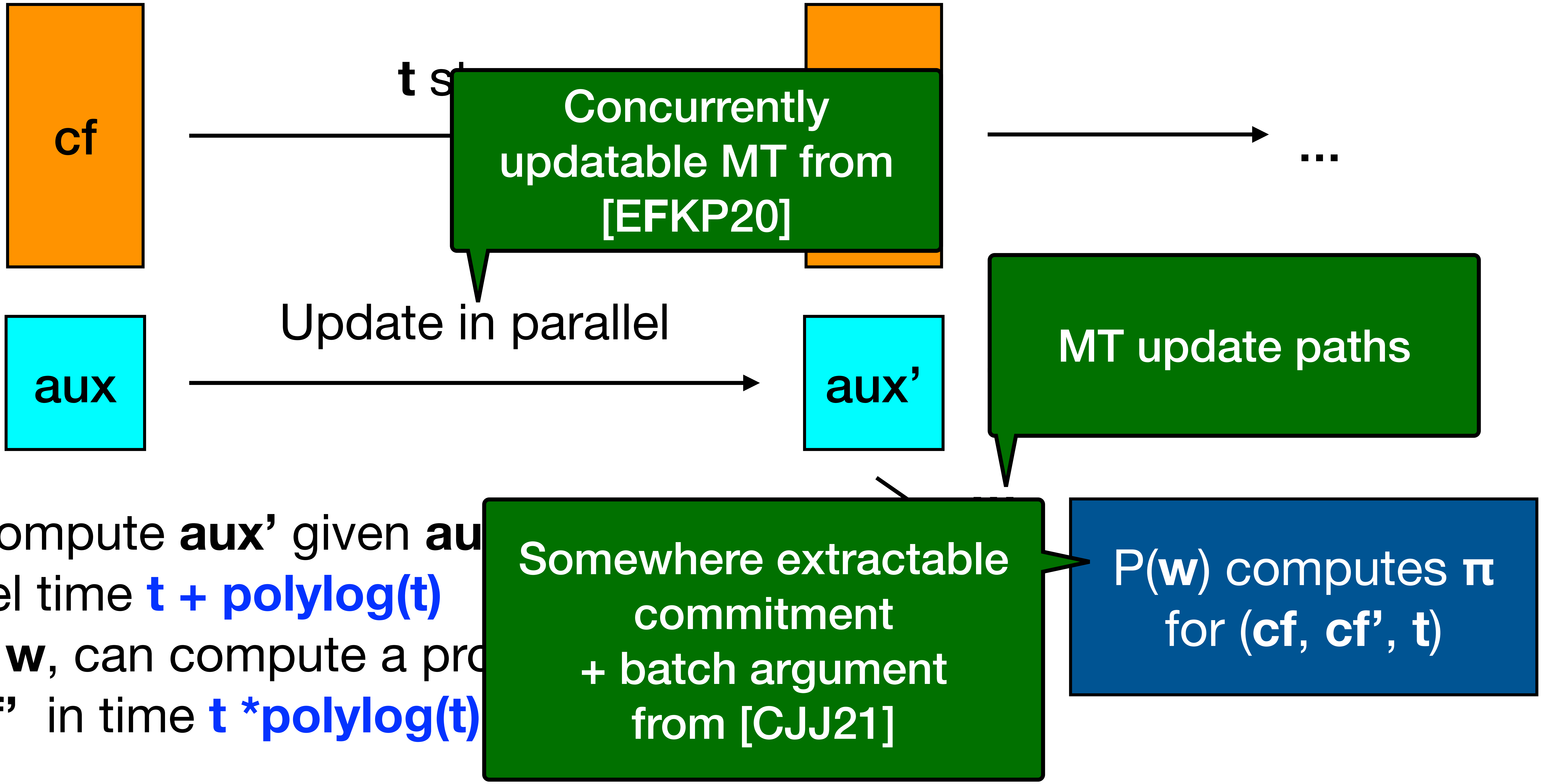
Instantiating from LWE



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  parallel time **t + polylog(t)**
- Given **w**, can compute a pr
  cf->cf' in time **t *polylog(t)**

Putting it all together with [EFKP20] transformation

Putting it all together with [EFKP20] transformation

Time: **0** —— **T**

Putting it all together with [EFKP20] transformation

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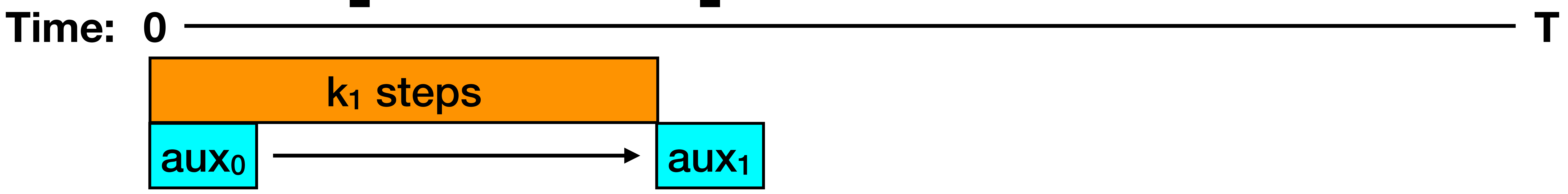
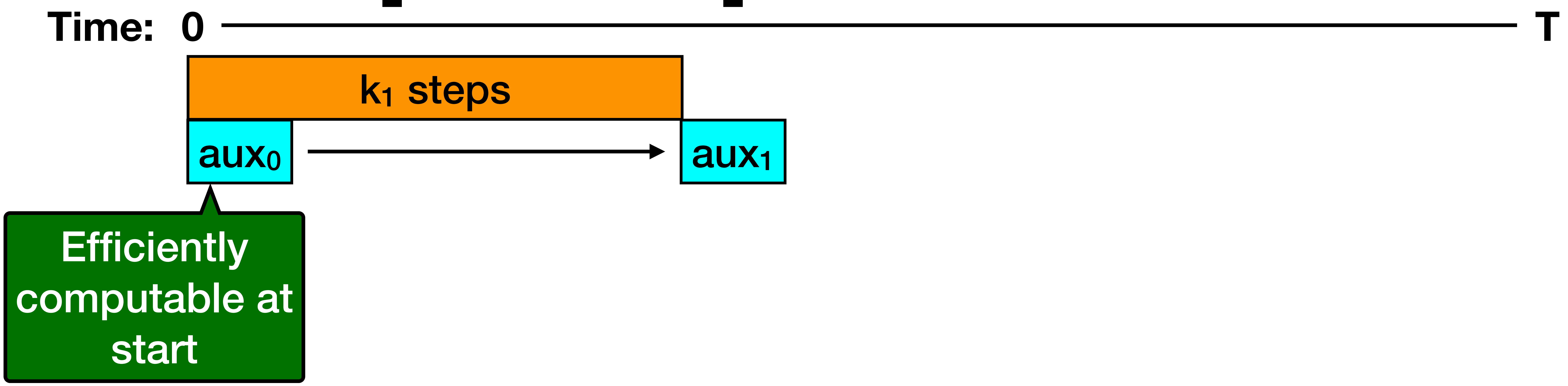


Putting it all together with [EFKP20] transformation



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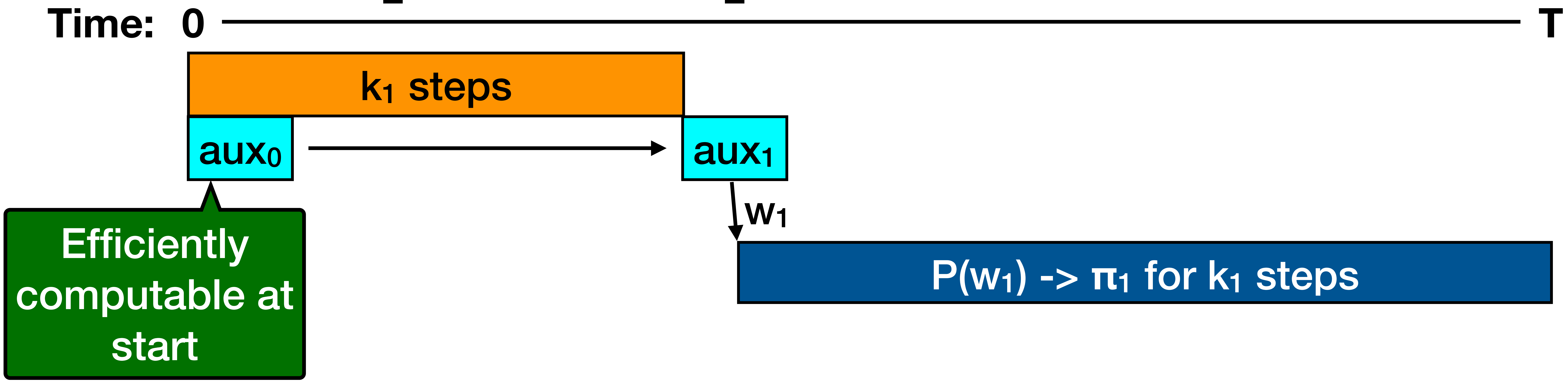

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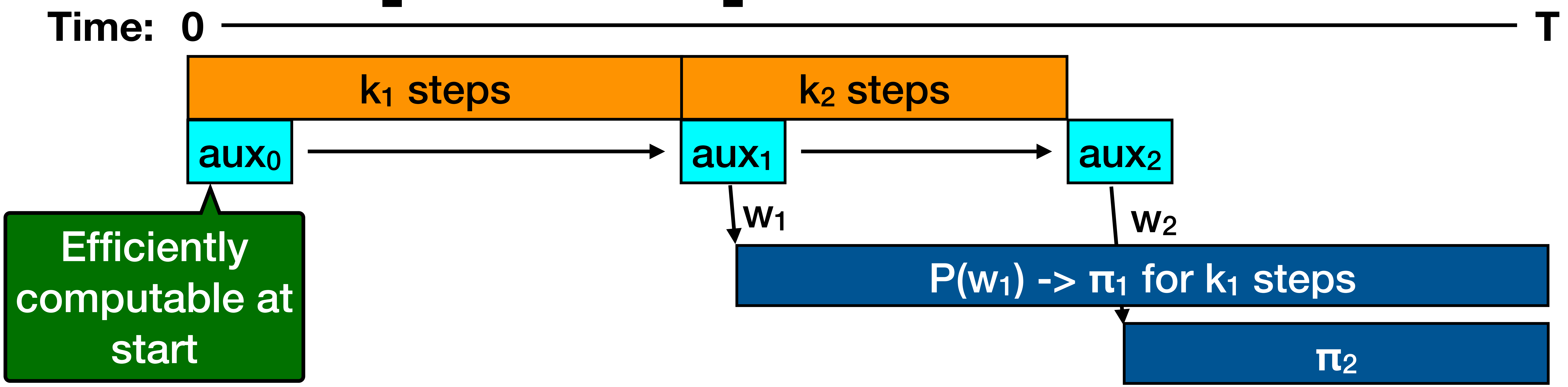
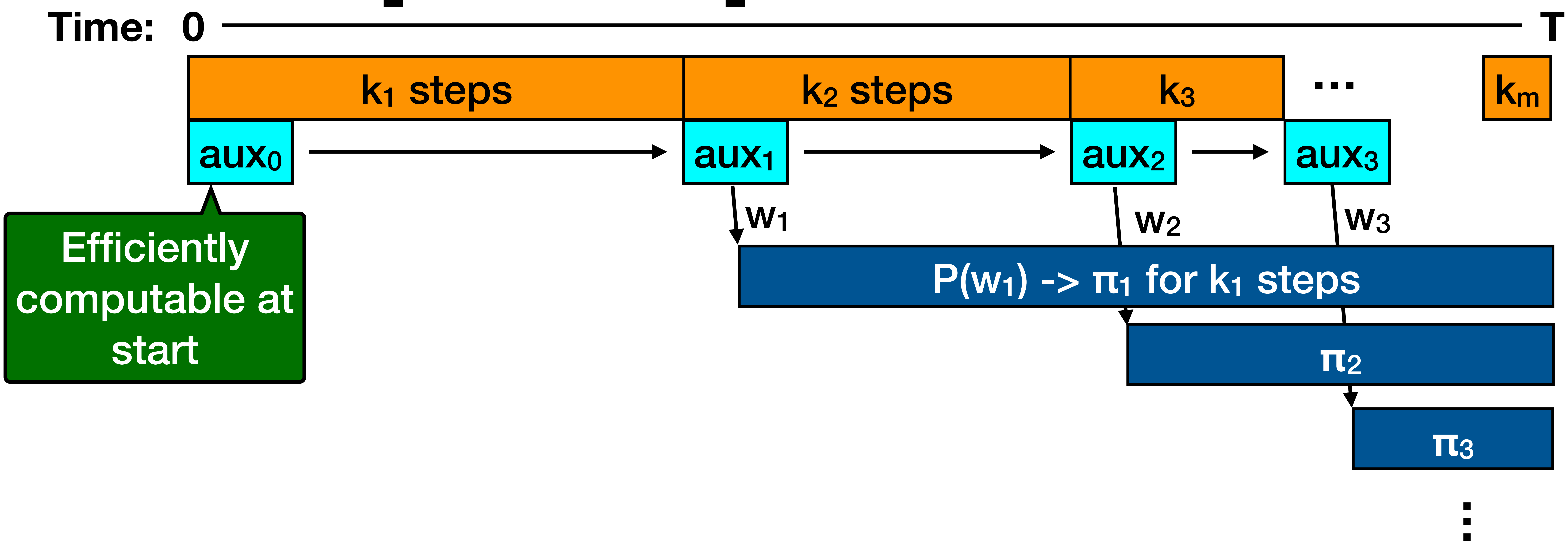
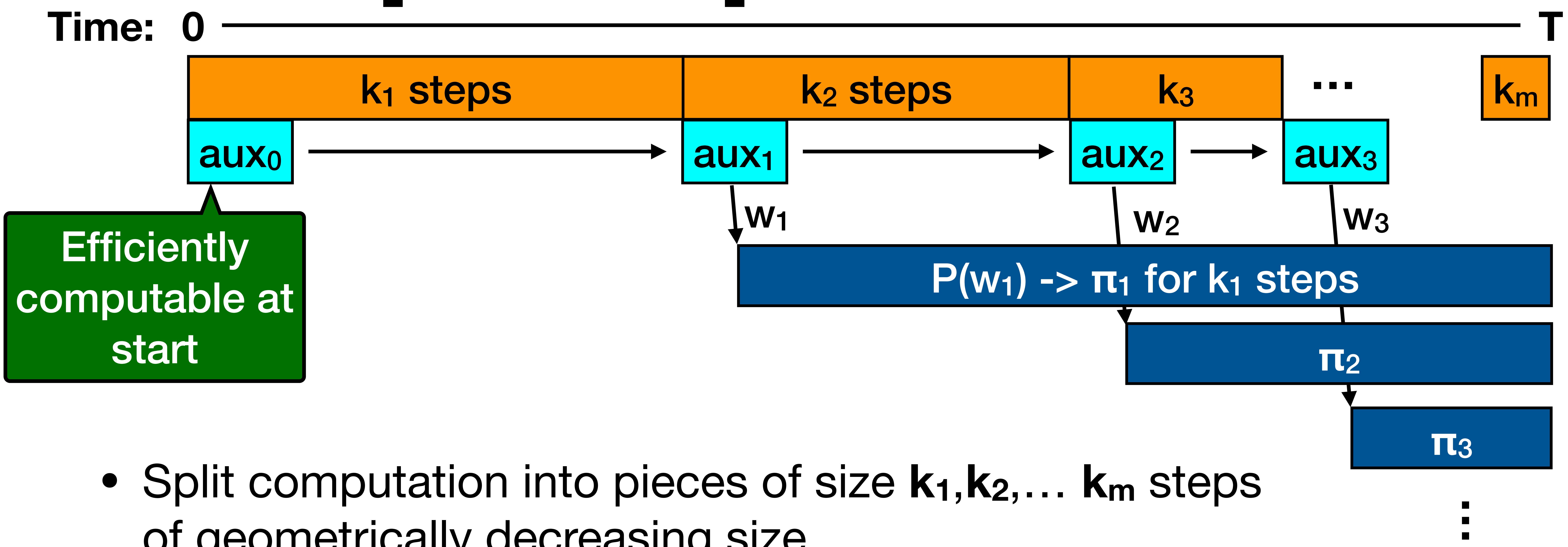


Putting it all together with [EFKP20] transformation

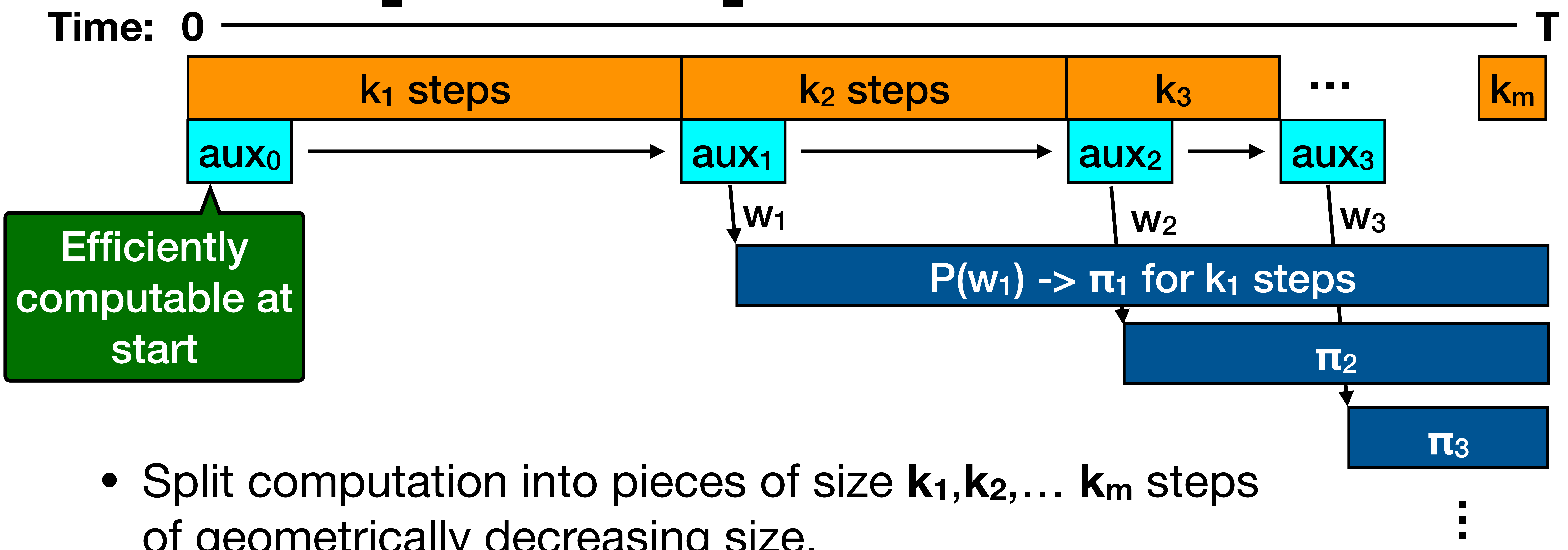


Putting it all together with [EFKP20] transformation



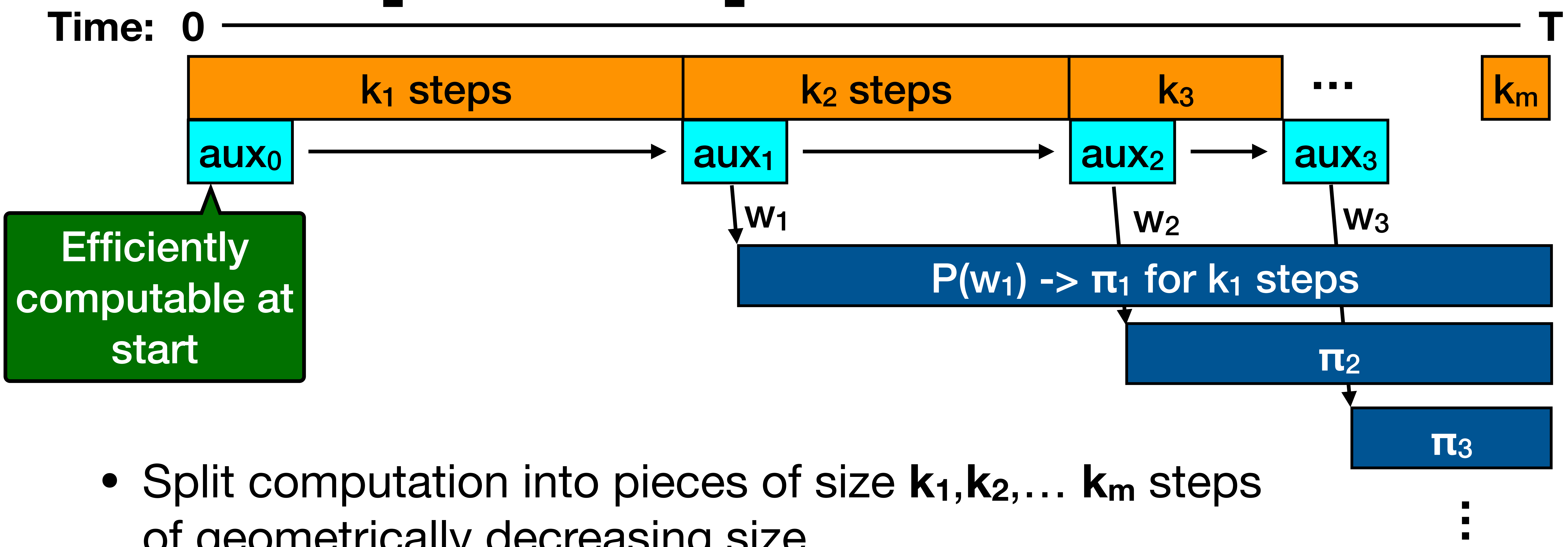
- Split computation into pieces of size $\mathbf{k_1}$,$\mathbf{k_2}$,… $\mathbf{k_m}$ steps of geometrically decreasing size.

Putting it all together with [EFKP20] transformation



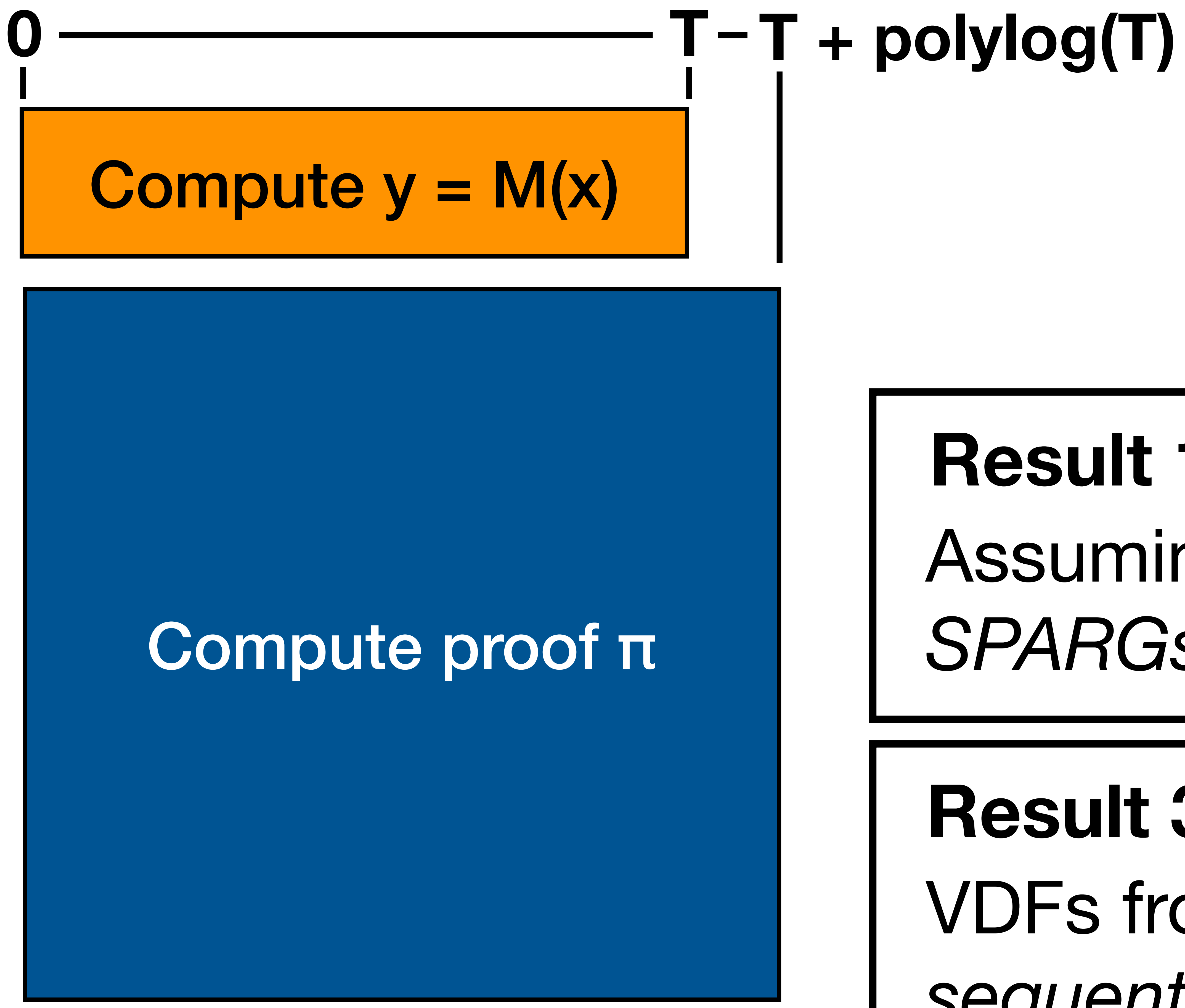
- Split computation into pieces of size $\mathbf{k_1},\mathbf{k_2},\ldots\ \mathbf{k_m}$ steps of geometrically decreasing size.
- Set $\mathbf{k_i}$ so that "i"th proof finished by time **T**.

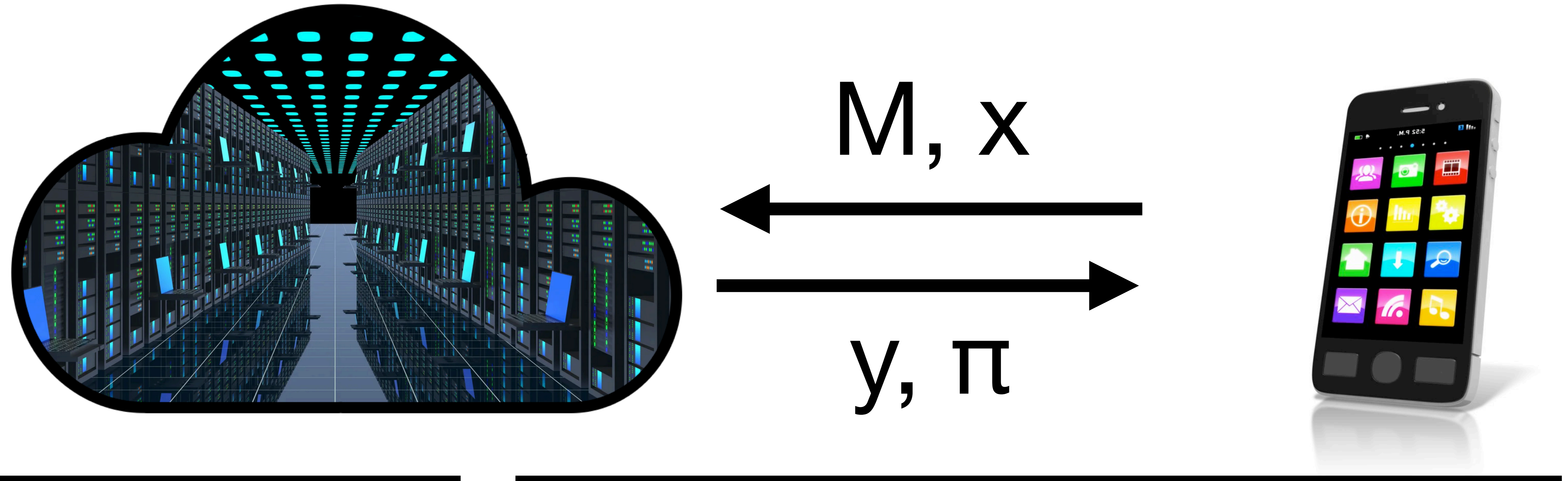
Putting it all together with [EFKP20] transformation



- Split computation into pieces of size $\mathbf{k_1}$,$\mathbf{k_2}$,… $\mathbf{k_m}$ steps of geometrically decreasing size.
- Set $\mathbf{k_i}$ so that "i"th proof finished by time **T**.
- Final proof consists of **m = polylog(T)** sub-proofs.

Questions?





Result 1:
Assuming *LWE*, exist *SPARGs for PRAM*.

Result 2:
SPARGs =>
time-independent SPARGs

Result 3:
VDFs from *LWE* + *any sequential function*

Result 4:
Mem-hard VDFs without "knowledge" assumptions