

RUHR-UNIVERSITÄT BOCHUM

# Composable Gadgets with Reused Fresh Masks - First-Order Probing-Secure Hardware Circuits with only 6 Fresh Masks

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## We've built a hardware gadget

- Enable the composition of any first-order (glitch-extended) robust secure circuit
- No gadget-individual fresh randomness necessary
- Only 6 fresh random masks in total
- Leads to randomness-optimized designs
- **COMAR** (Composable Gadgets with Reused fresh Masks)

## Masking on an algorithmic Level

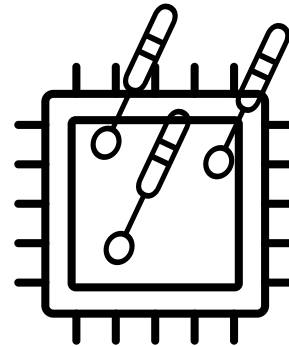
- Requires high expertise
- Prone to errors
- Often no formal security proof
- Leads to optimized designs

## Gadget-based Masking

- Based on composability notions
- Can be automated
- Leads to provable secure designs
- Usually introduces higher overhead

## The ISW d-probing model

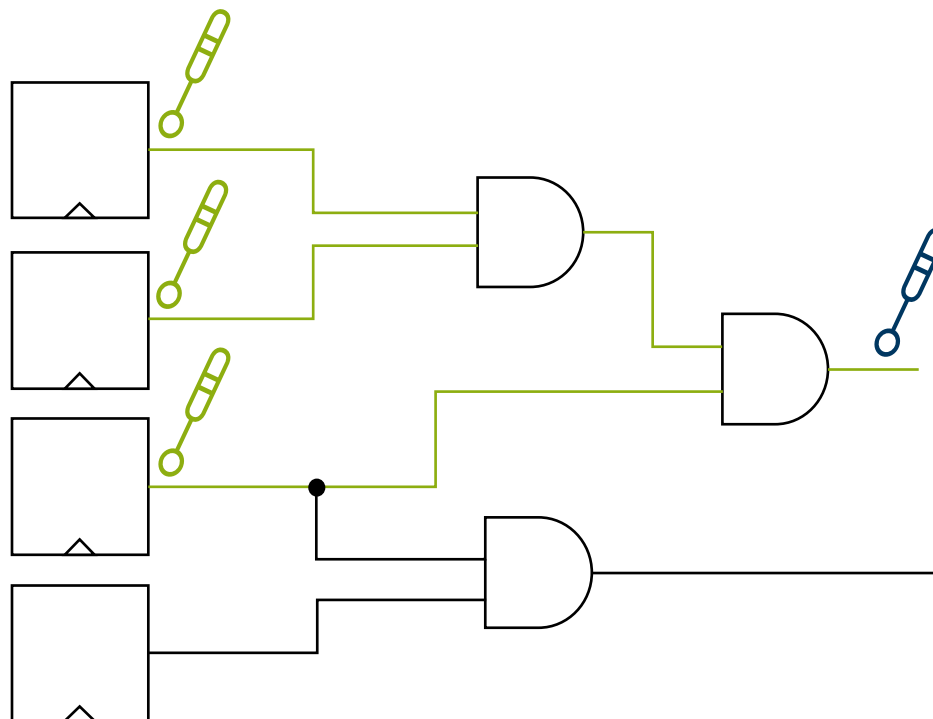
- Offers high abstraction
- Existing reduction into the *Noisy Leakage Model* (which is close to the real world)
- Extension to HW: robust d-probing Model



Standard probe



Extended probe



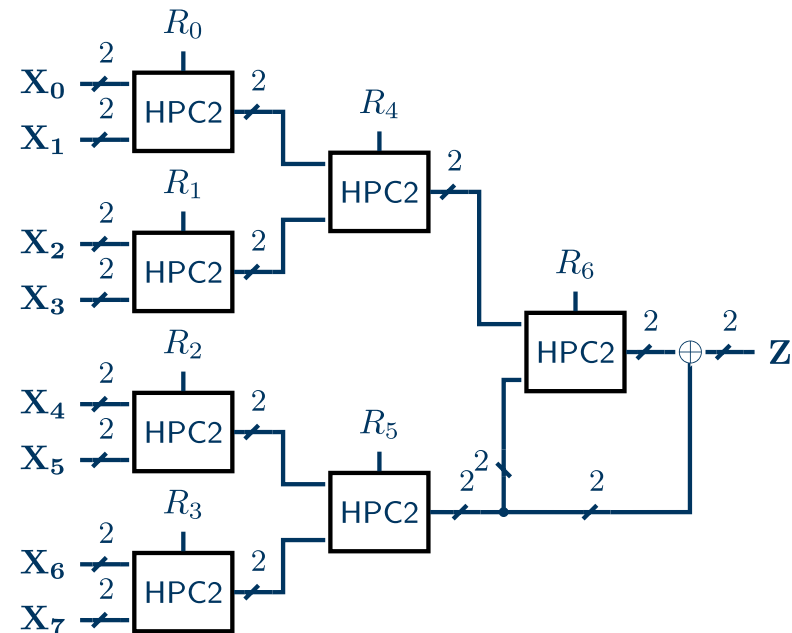
## Why is our work important?

### Composable gadgets are typically realizing atomic gates

- AND, OR, NAND, NOR, ...

### This introduces individual randomness overhead per gadget

- Results in high overall overhead w.r.t. the randomness requirements



# RESEARCH QUESTION

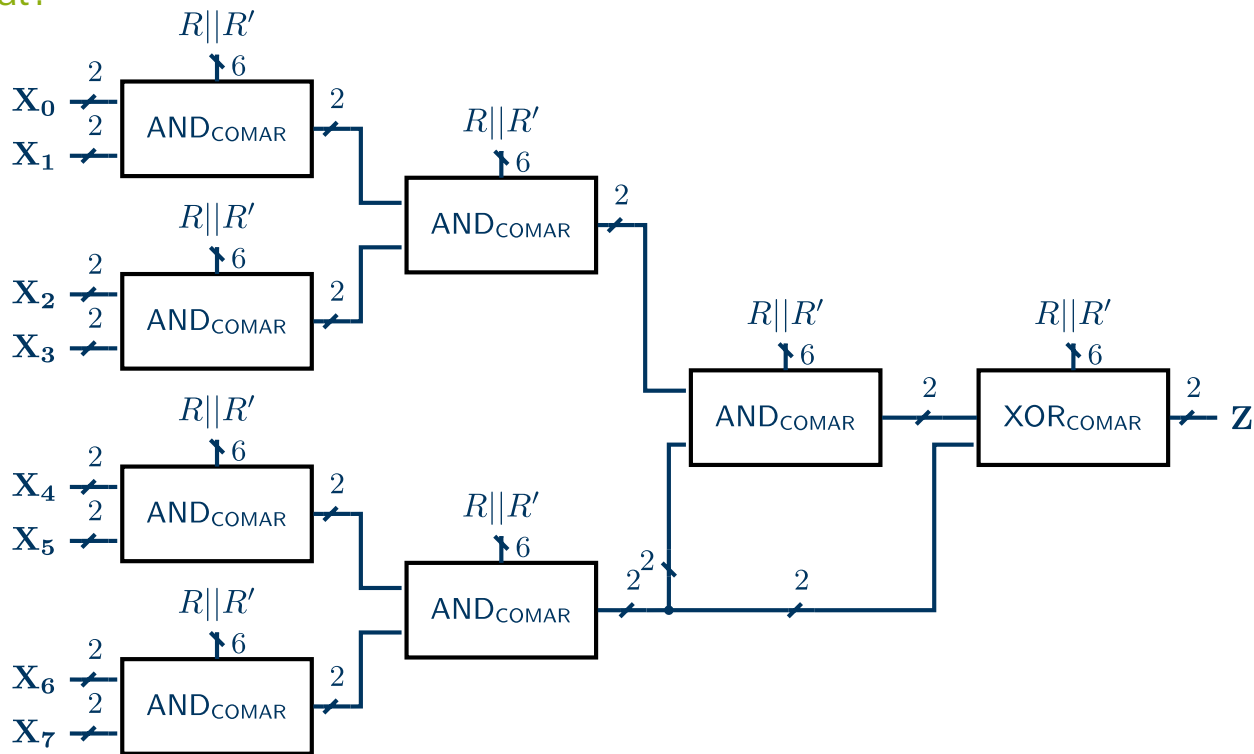
What was the goal?



Can we build gadgets where we can re-use the same randomness in every gadget?

# RESEARCH QUESTION

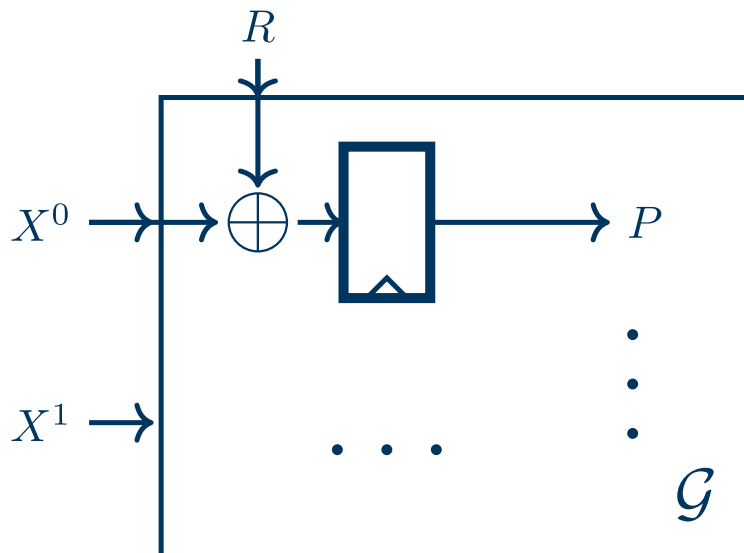
What was the goal?

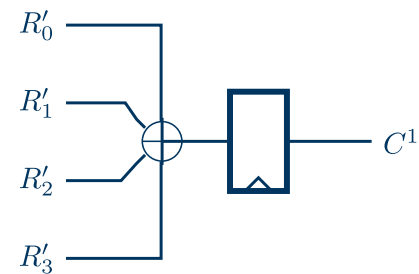
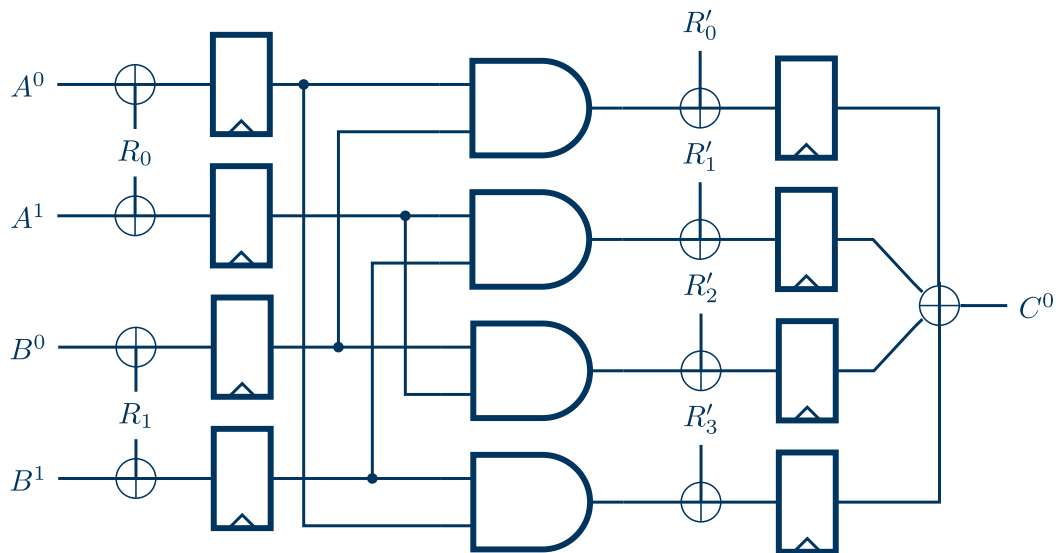


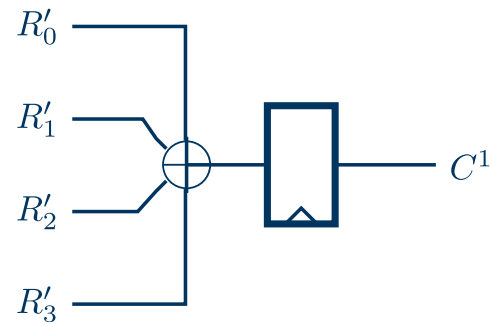
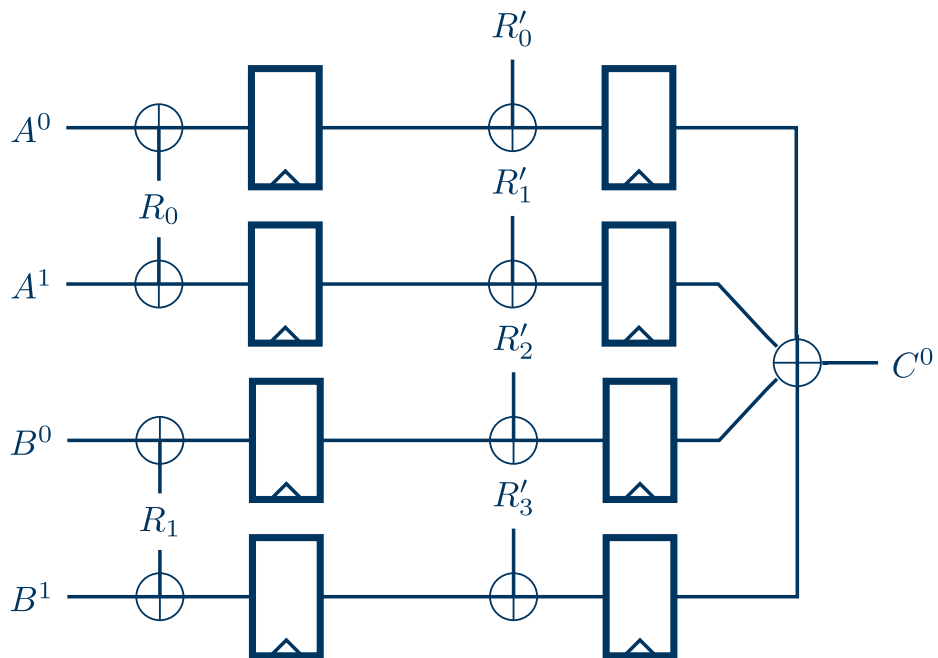


## Why is fresh randomness necessary?

Gadget-individual fresh mask allow to argue about simulatability of probes within a gadget because the input is independent of any other fresh mask.







# ARBITRARY INPUT WIDTH

We can extend our 2-input gadgets



## We also constructed n-input ANDs

- and all other non-linear gates which can easily be derived from AND
- $n + 2^n$  fresh masks are needed for the whole circuit.**
- Here  $n$  is the maximal input width used within the circuit.

## The randomness requirements are drastically improved by our approach

- Breakeven point compared to for example HPC2 is 6 AND gates

## Additional latency is the price we pay here

- XOR is not for free w.r.t. latency as for example in the PINI framework

## Multiple-input gadgets mitigate this disadvantage

Scheme	Fresh Random	Latency [cycle]		Critical Path	Area
	[bit/cycle]	added	full	Delay [ns]	[GE]
<b>AES-128</b>					
HPC2	680	8	99	2.04	52 597
GHPC	680	8	99	1.48	67 193
GHPC <sub>LL</sub>	2720	4	55	2.28	52 450
COMAR	6	42	473	1.23	140 214
<b>Skinny64-64</b>					
HPC2	64	4	165	0.55	6 895
GHPC	64	2	99	0.80	22 850
GHPC <sub>LL</sub>	1024	1	66	0.85	18 705
COMAR	6	22	759	0.58	22 090

Scheme	Area [GE]		
	LFSR 31-bit	LFSR 64-bit	Keccak, Variant
<b>AES-128</b>			
HPC2	247 281	437 205	409 195, [800]
GHPC	261 673	451 393	423 791, [800]
GHPC <sub>LL</sub>	830 370	1 589 250	1 557 778, [1600]×2
COMAR	141 932	143 608	144 534, [25]
<b>Skinny64-64</b>			
HPC2	25 218	43 093	82 009, [200]
GHPC	41 154	59 010	97 964, [200]
GHPC <sub>LL</sub>	311 569	597 265	771 369, [1600]
COMAR	23 808	25 483	26 410, [25]



Thanks!  
Any Questions?

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