Riding the Waves Towards Generic Single-Cycle Masking in Hardware

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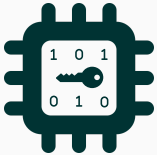
Motivation

Power analysis attacks pose a threat to real-world crypto implementations.



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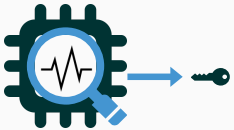

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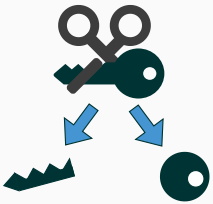

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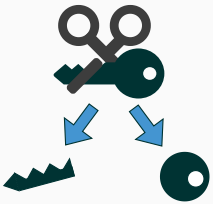
- Glitches from combinatorial circuits can reveal cryptographic secrets.



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Low Latency Masking

Can we implement masked circuits which compute (securely) in a single clock cycle?

Self-Synchronized Masking

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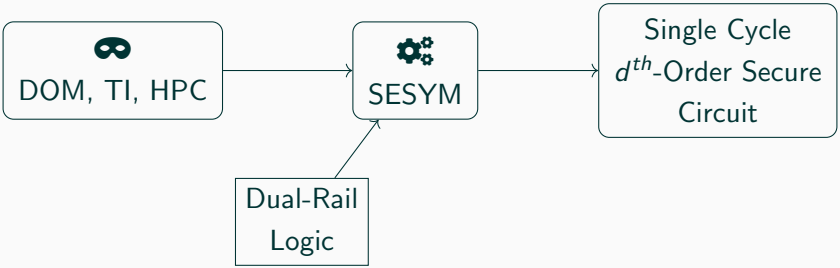

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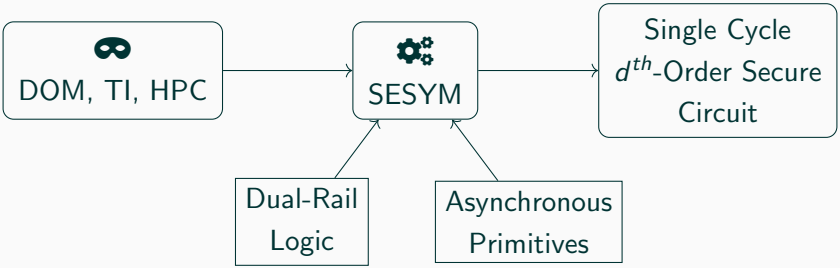
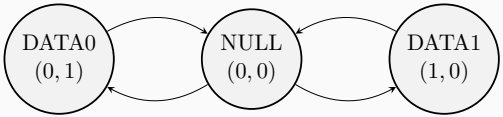
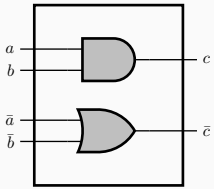


Dual-Rail Logic

- Use two wires to encode a bit
- Dual-rail logic is evaluated in two steps:
  1. Precharge - Drive all wires from DATA to NULL
  2. Evaluate - Compute NULL to DATA



Wave Dynamic Differential Logic (**WDDL**) is a dual-rail logic style based on standard cells.



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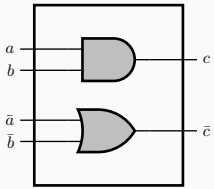

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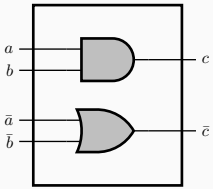

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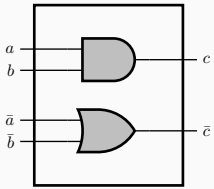
→ WDDL gates do not glitch [TV04].



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Asynchronous Primitive – Muller C-element [Mul56]

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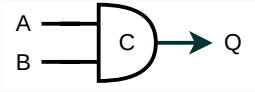


(a) Symbol

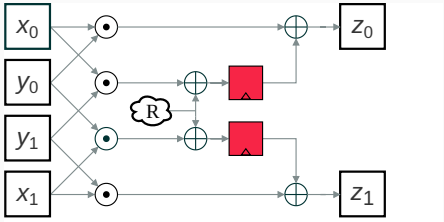
A	B	Q
0	0	0
0	1	-
1	0	-
1	1	1

(b) Truth Table

Designing with SESYM

Applying SESYM on a 1^{st}-order DOM AND gate

The 1^{st}-order DOM AND gate requires two clock cycles to compute due to the registers. Can we remove them?



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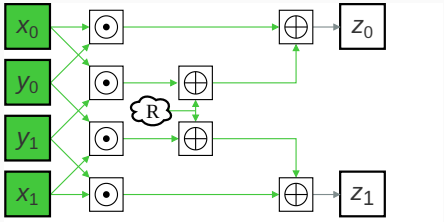

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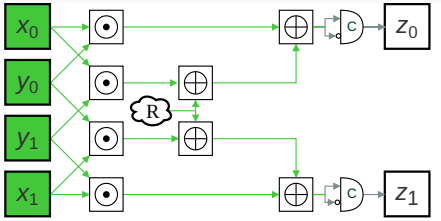
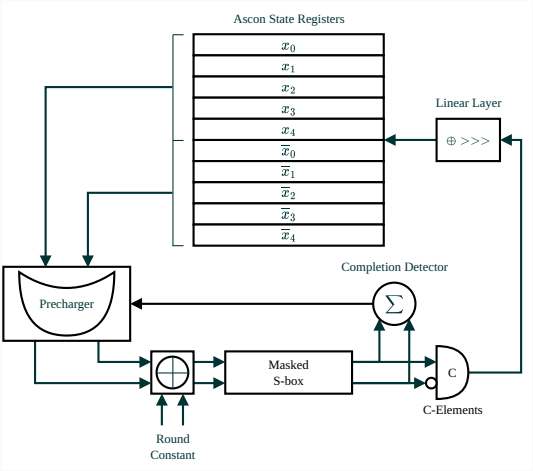
2. Insert C-elements to latch the computed result and convert back to single-rail.



Applying SESYM to the Ascon Permutation



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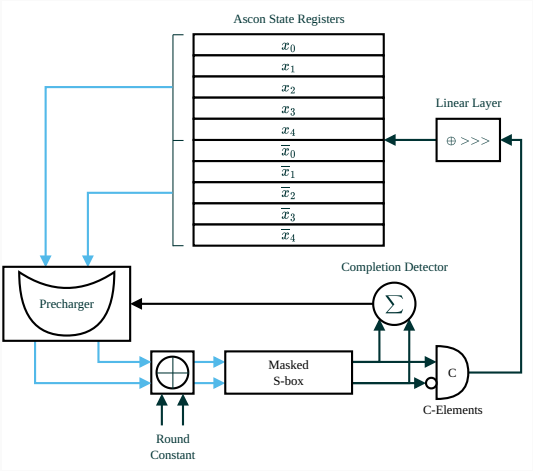

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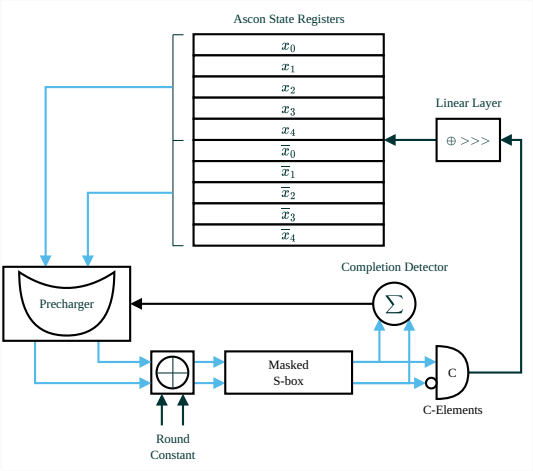

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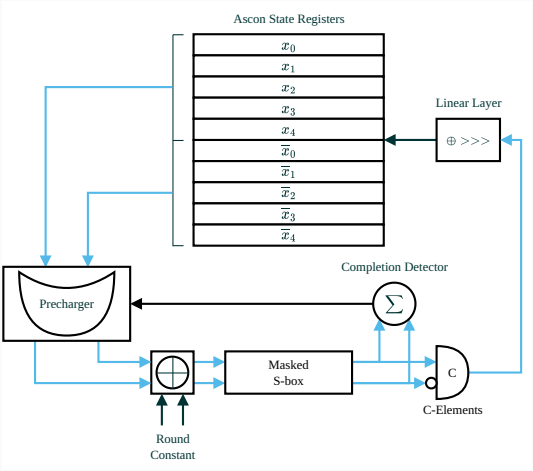

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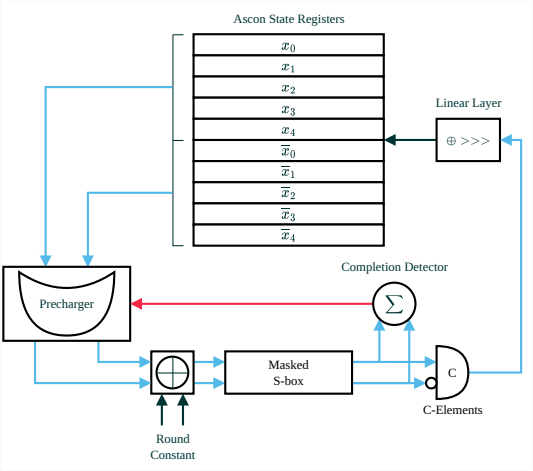

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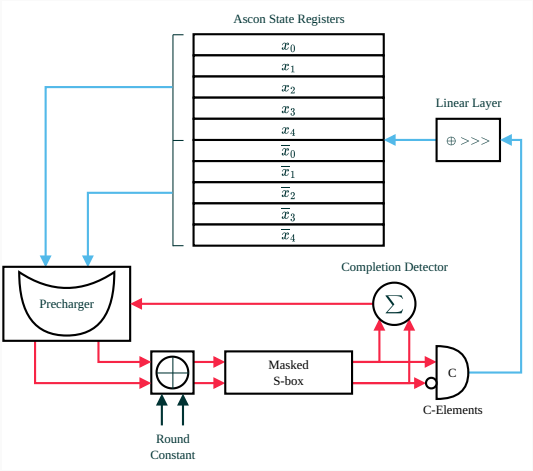

Implementations

Ascon Implementation Results

Protection Order	Area [kGE]	Cycle/round [cycle]	Randomness [bits/cycle]	Max Clock Freq. MHz
This Work, UMC65nm				
1	50.40	1	320	408.3
2	102.39	1	960	377.1
3	172.05	1	1 920	358.4
4	257.13	1	3 200	334.2
5	357.65	1	4 800	312.9
GLM, UMC90nm [GIB18]				
1	42.59	1	2 048	260.0
2	90.78	1	4 608	-
3	153.76	1	8 192	-
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[Sas+20]	LMDPL	3.48	1	36
This work	**SESYM-BP**	**3.98**	**1**	**34**
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AES-128 Implementations

Impl.	Protection Order	Area [kGE]	Cycle/round [cycle]	Randomness [bits/cycle]	Max Clock Freq. [MHz]
This work	**1**	**104.86**	**1**	**680**	**192.3**
This work	**2**	**203.90**	**1**	**2040**	**169.2**
[Sas+20]	1	157.50	1	976	400

Security Evaluations

Coco [Gig+21] formally verifies the security of a circuit against power analysis attacks while taking glitches and transitions into account.

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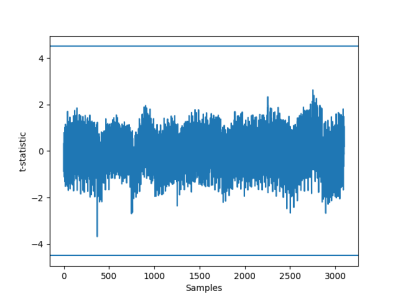
Coco successfully verified:

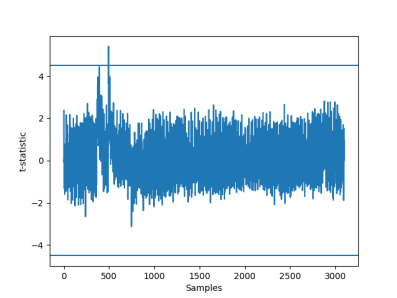
- ✔ 1^{st}-order & 2^{nd}-order Ascon S-box.
- ✔ 1^{st}-order & 2^{nd}-order AES-BP S-box.

We implemented our designs onto a CW305 (Artix-7 FPGA) and performed physical side-channel evaluations.

1^{st}-order ASCON Impl. – 10 Million traces.

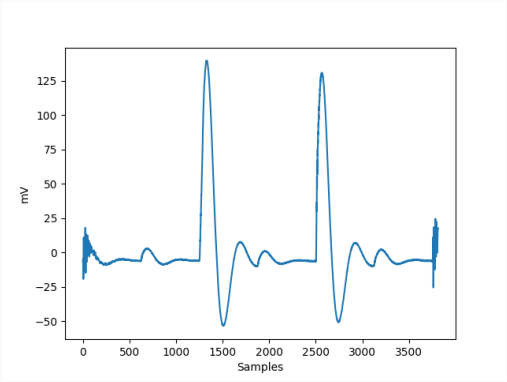


1^{st}-order t-test

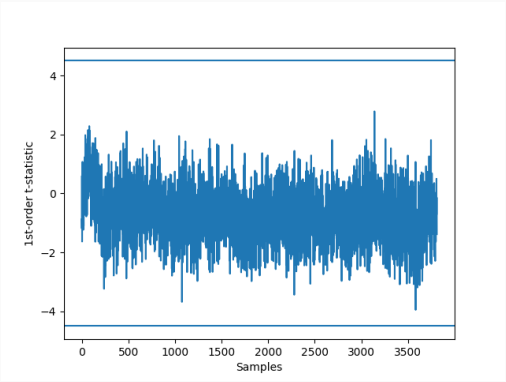


2^{nd}-order t-test

2^{nd}-order AES-Canright – 100 Million traces i

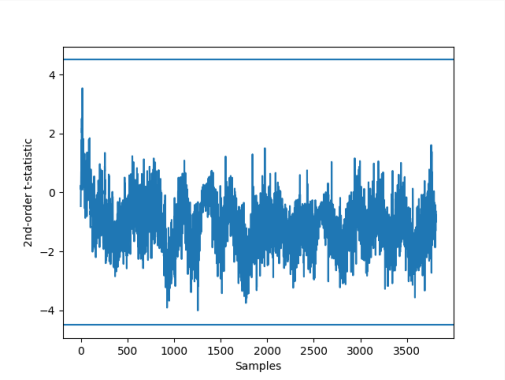


Average Power trace.

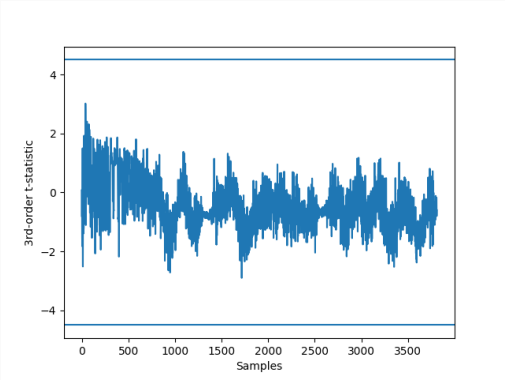


1^{st} order t-test

2^{nd}-order AES-Canright – 100 Million traces ii

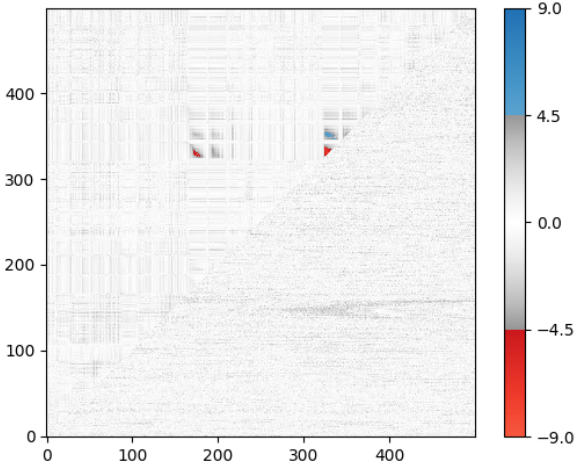


2^{nd} order t-test



3^{rd} order t-test

2^{nd}-order AES-Canright – Bivariate, 10 Million traces



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References

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