eLIMInate: a Leakage-focused ISE for Masked Implementation

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05/09/24

Context (1)

- Problem: leakage stemming from the **overwriting effect** (see, e.g., [13, Section 3.1])

$$\begin{array}{l} \vdots \\ \mathsf{GPR}[x] \longleftarrow v_i \\ \vdots \\ \mathsf{GPR}[x] \longleftarrow v_j \quad \rightsquigarrow \Lambda \simeq \mathrm{HD}(v_i, v_j) \\ \vdots \end{array}$$

which is an issue if v_i and v_j are Boolean shares of some underlying v.

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$$
\begin{array}{lcll}
 & \vdots & & \\
\mathsf{GPR}[x] & \longleftarrow & v_i & \\
 & \vdots & & \\
\mathsf{GPR}[x] & \longleftarrow & 0 & \rightsquigarrow \Lambda \simeq \mathrm{HD}(v_i, 0) \\
\mathsf{GPR}[x] & \longleftarrow & v_j & \rightsquigarrow \Lambda \simeq \mathrm{HD}(0, v_j) \\
 & \vdots & &
\end{array}
$$

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- Approach #1: alter software implementation to eliminate such overwriting, e.g.,
  1. "flush" resource by pre-zero'ing it,
  2. select different resource allocation,
  3. ...

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  2. select different resource allocation,
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- Challenge(s):
  1. modulo automation (e.g., Rosita [14, 15]), challenging re. scale, complexity, etc.,
  2. some, e.g., micro-architectural resources cannot be explicitly controlled,
  3. a secure solution may be inefficient,
  4. ...

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- Approach #2: task hardware, i.e., the micro-architecture with overwriting elimination.
- Challenge(s):
  1. per Gigerl et al. [8, Section 3], "*[w]hile fixing such [overwriting] problems in hardware would, in principle, be possible, it would be very costly*",
  2. the ISA prevents knowledge of, e.g., security-critical vs. security-agnostic operands.

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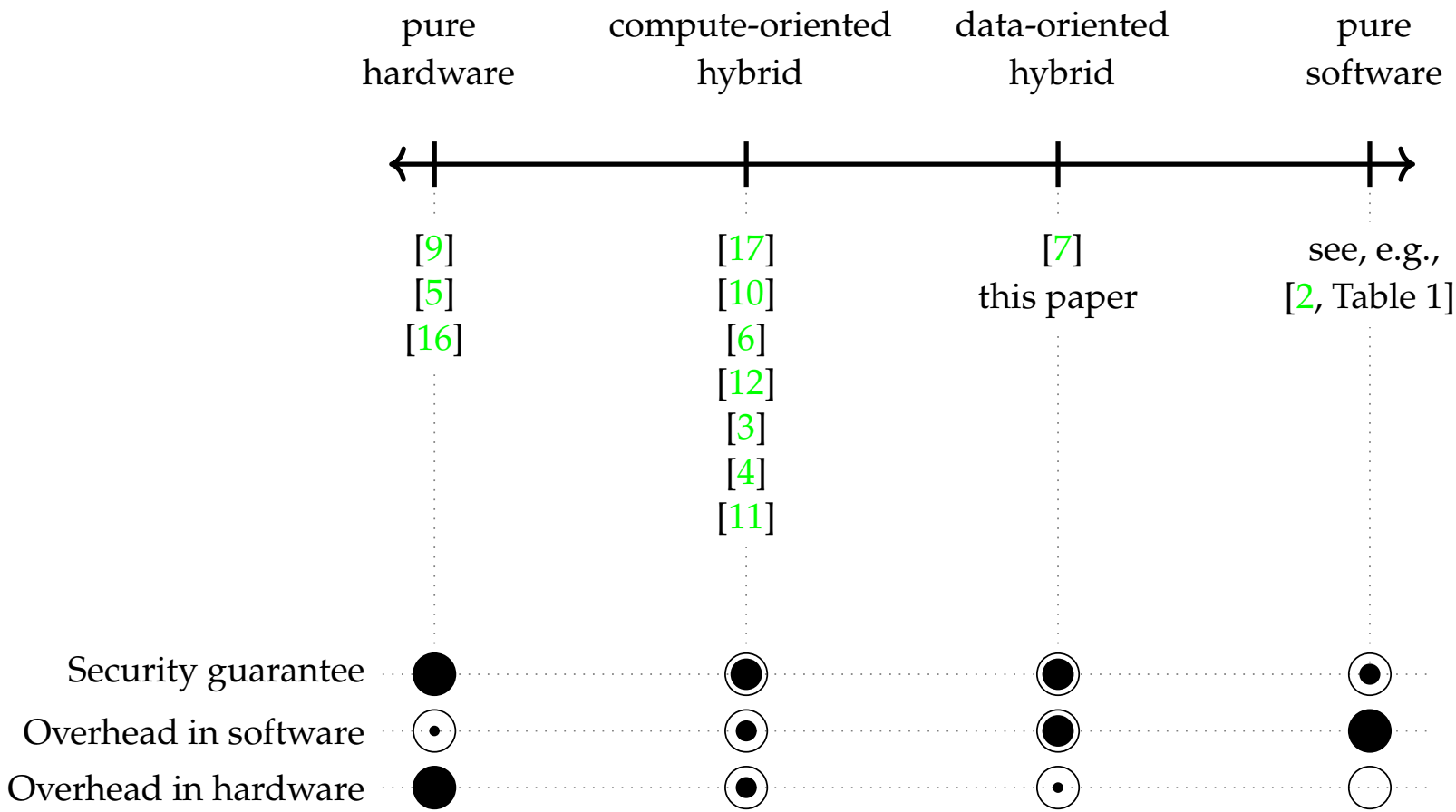
  which is an issue if v_i and v_j are Boolean shares of some underlying v.
- Approach #3: hardware/software co-design, i.e., an ISE ...

Context (2)

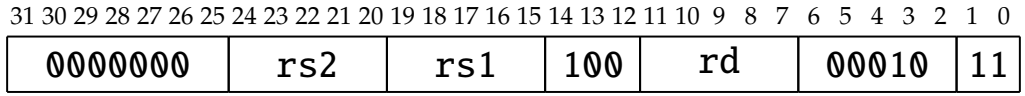
- ... an aside: there's a large design space of approaches related to masking, e.g.,



eLIMInate'ing (only) overwriting-based leakage (1)

- Design:
  - base ISA is RV32I,
  - class-1 instructions: *computation*-related, e.g.,

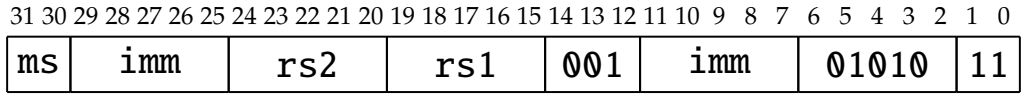
`sec.xor rd, rs1, rs2` :



$$\mapsto \quad \texttt{GPR[rd]} \overset{\Delta}{\longleftarrow} \texttt{GPR[rs1]} \oplus \texttt{GPR[rs2]}$$

  - class-2 instructions: *storage*-related, e.g.,

`sec.sw rs2, rs1, imm, ms` :



$$\mapsto \quad \texttt{MEM[GPR[rs1]} + \texttt{imm]}^4 \overset{\Delta}{\longleftarrow} \texttt{GPR[rs2]}$$

i.e.,

- $\overset{\Delta}{\longleftarrow}$ vs. $\longleftarrow$ denotes a "hint" to eliminate overwriting (noting flexibility re. implementation),
- otherwise functional semantics remain the same,
- so *ideal* outcome is change from, e.g., `xor` to `sec.xor` and that's it.

eLIMInate'ing (only) overwriting-based leakage (2)

- Implementation:
  - base core is (vanilla) Ibex,
  - implementation #1: latency-optimised.

$$\begin{array}{lcl} \text{class-1 instructions} & \simeq & \text{double-buffer} \\ \text{class-2 instructions} & \simeq & \text{mask/unmask at egress/ingress} \end{array}$$

  - implementation #2: area-optimised.

$$\left.\begin{array}{l} \text{class-1 instructions} \simeq \\ \text{class-2 instructions} \simeq \end{array}\right\} \text{double-step (cf. pre-charge then evaluate)}$$

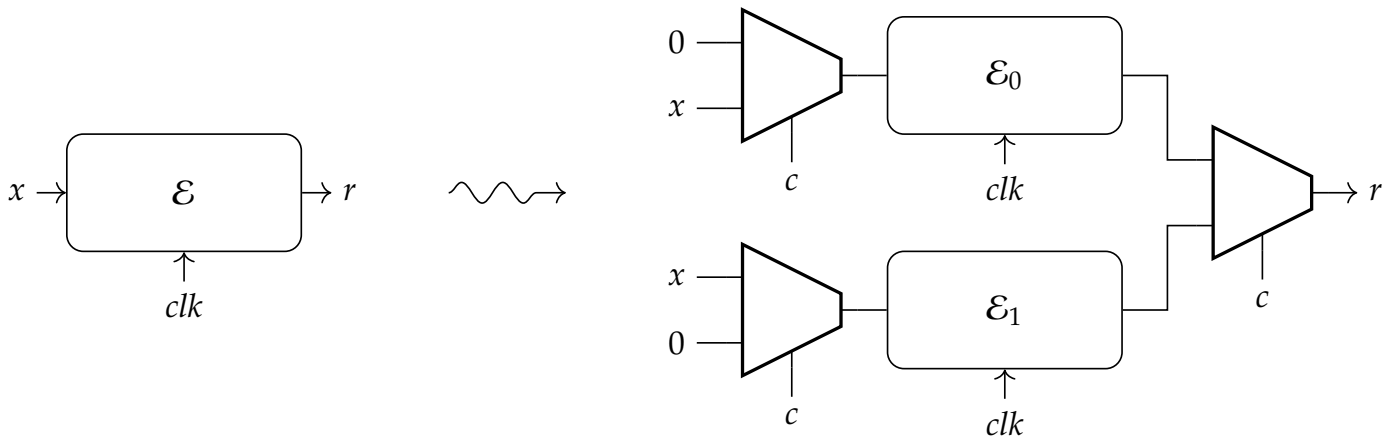
  noting that
  - both adopt conservative assumption re. extra-core resources,
  - latency-optimised class-2 instructions depend on state, i.e., CSRs, indexed by `ms` field.

eLIMInate'ing (only) overwriting-based leakage (3)

- Implementation: latency-optimised, class-1.
  - example instruction:

```
sec.xor x1, x2, x3
```

  - (general-purpose) option #1: double-buffer



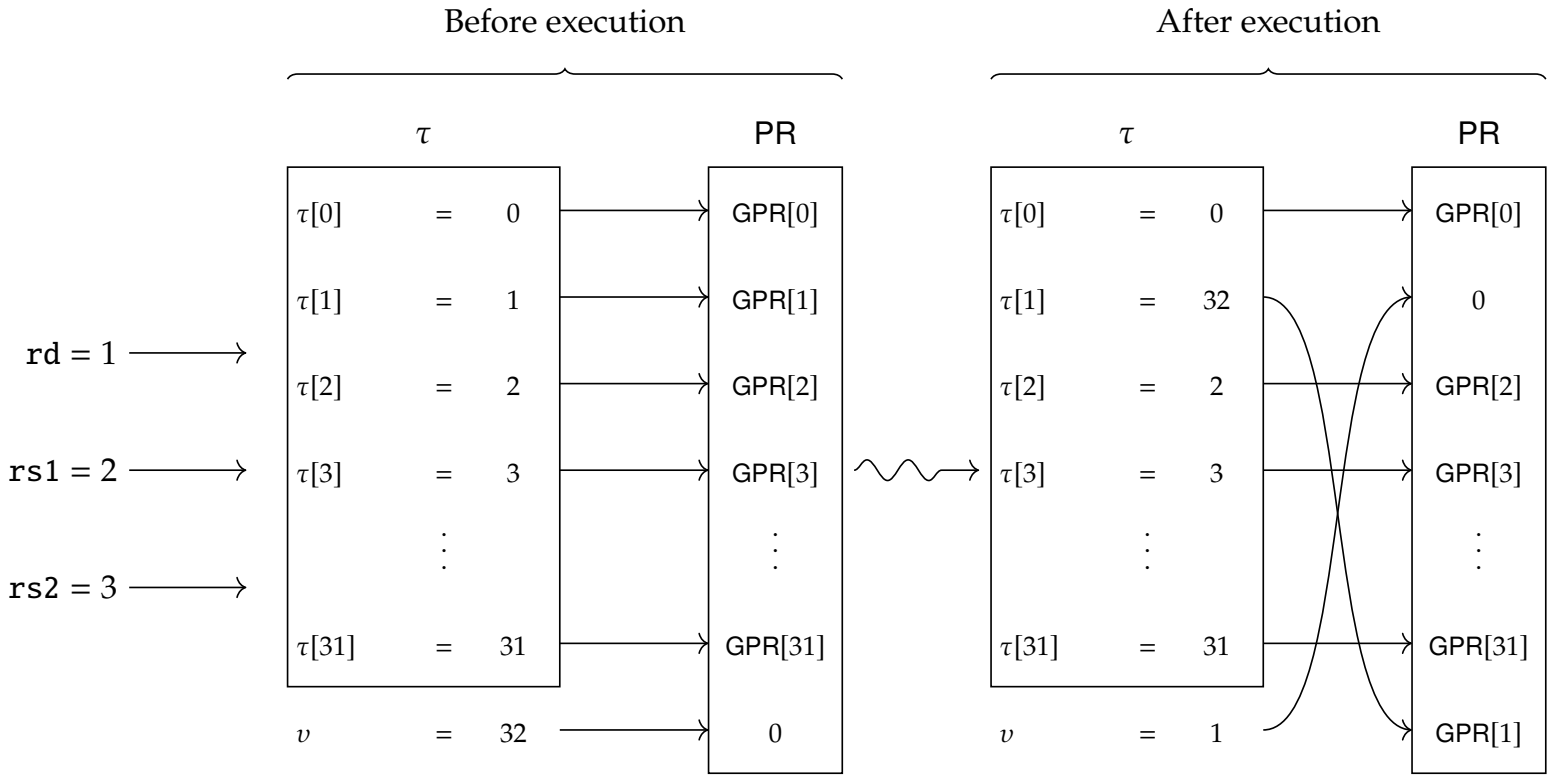
for isolated registers.

eLIMInate'ing (only) overwriting-based leakage (3)

- Implementation: latency-optimised, class-1.
  - example instruction:

```
sec.xor x1, x2, x3
```

  - (special-purpose) option #2: light-weight register renaming



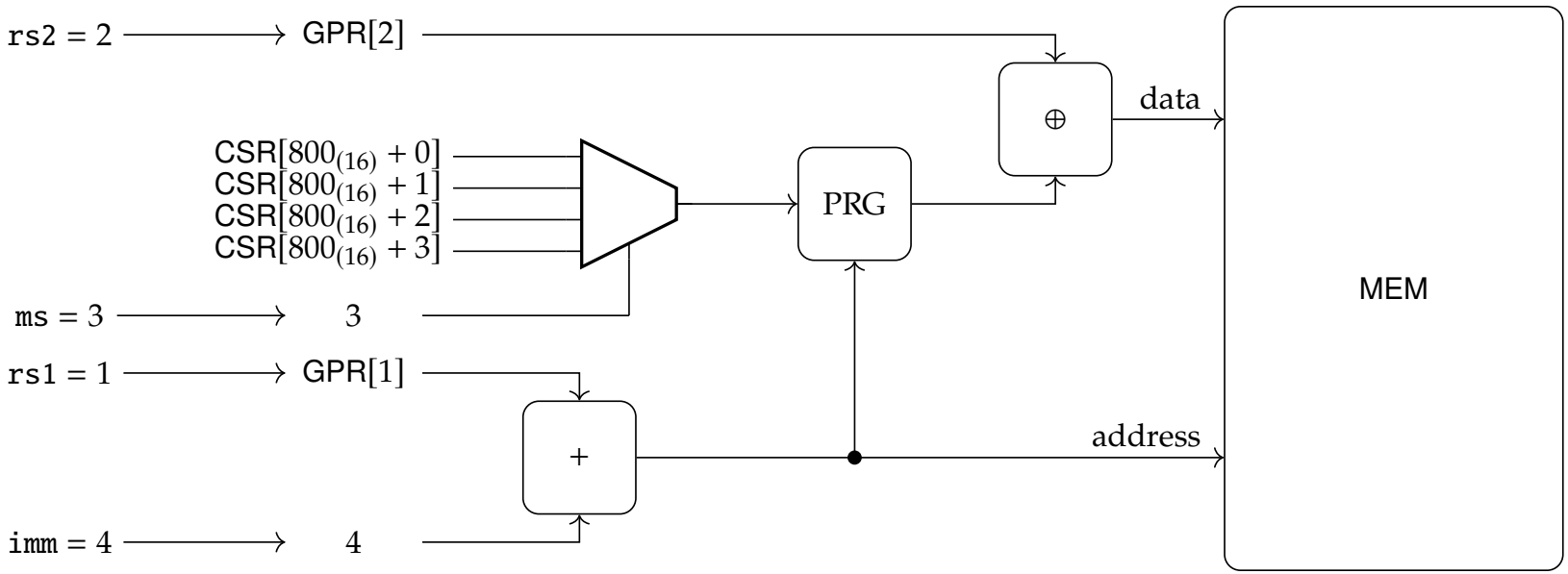
for register file.

eLIMInate'ing (only) overwriting-based leakage (4)

- Implementation: latency-optimised, class-2.
  - example instruction:

```
sec.sw x2, x1, 4, 3
```

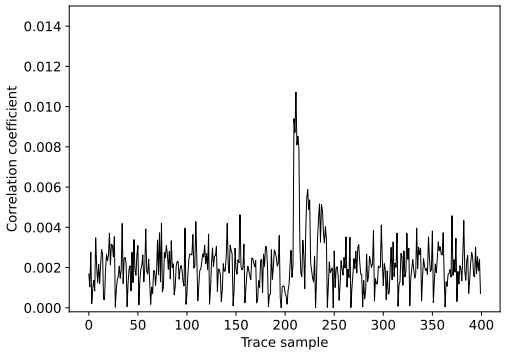
  - executed per



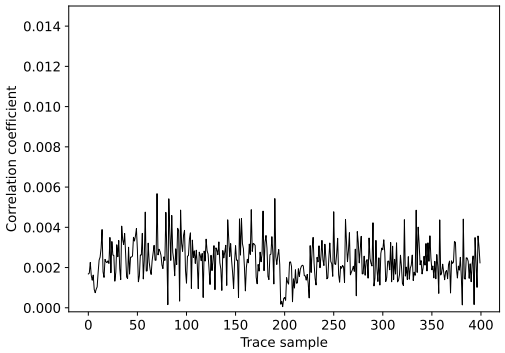
i.e., address-specific *re*masking, so basically the same as [5, Section 4].

eLIMInate'ing (only) overwriting-based leakage (5)

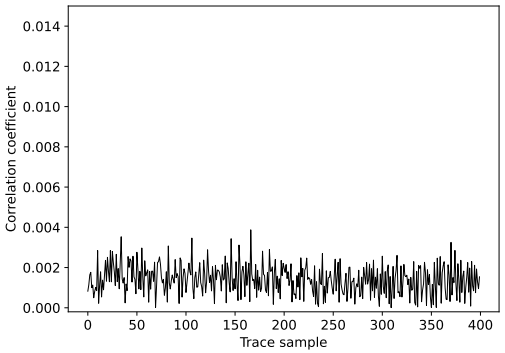
- Evaluation: based on CW305, so Xilinx Artix-7 FPGA.
  1. security-oriented:
     - experimental evidence CPA-based [1] leakage evaluation, e.g.,



`xor`



`sec.xor`
latency-opt.



`sec.xor`
area-opt.

     plus
     - analytical evidence from CoCo-based [8] verification.

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https://www.newae.com/products/nae-cw305

eLIMInate'ing (only) overwriting-based leakage (5)

- Evaluation: based on CW305, so Xilinx Artix-7 FPGA.

2. efficiency-oriented:
   - area:

	Registers	LUTs
Base core	2364 (1.00×)	3722 (1.00×)
Base core + latency-opt. class-1	2585 (1.09×)	4950 (1.33×)
Base core + latency-opt. class-1+2	2713 (1.15×)	5242 (1.41×)
Base core + area-opt. class-1	2363 (1.00×)	3710 (1.00×)
Base core + area-opt. class-1+2	2364 (1.00×)	3877 (1.04×)

   - latency:

	`[sec.]and`	`[sec.]andi`	`[sec.]or`	`[sec.]ori`	`[sec.]xor`	`[sec.]xori`	`[sec.]slli`	`[sec.]srli`	`[sec.]add`	`[sec.]sub`
Base core	1	1	1	1	1	1	1	1	1	1
Base core + latency-opt. class-1	1	1	1	1	1	1	1	1	1	1
Base core + area-opt. class-1	2	2	2	2	2	2	2	2	2	2

	`[sec.]lw`	`[sec.]sw`	`[sec.]lbu`	`[sec.]sb`
Base core	2	2	2	2
Base core + latency-opt. class-2	2	2	2	2
Base core + area-opt. class-2	6	4	6	4

https://www.newae.com/products/nae-cw305

Conclusions

- Take away points:
  - we pitch eLIMInate more as an exploration than a solution per se,
  - a high-level summary would be

$$\text{latency-optimised} \quad \rightsquigarrow \quad \begin{cases} \text{less} & \text{latency} & \text{overhead} \\ \text{more} & \text{area} & \text{overhead} \\ \text{more} & \text{usability} & \text{overhead} \\ \text{more} & \text{robust} & \end{cases}$$

$$\text{area-optimised} \quad \rightsquigarrow \quad \begin{cases} \text{more} & \text{latency} & \text{overhead} \\ \text{less} & \text{area} & \text{overhead} \\ \text{less} & \text{usability} & \text{overhead} \\ \text{less} & \text{robust} & \end{cases}$$

  with robustness relating to class-2, so *extra*-core resources.

Conclusions

- Take away points:

- in more detail/depth:
  - a more general leakage elimination hint is an attractive idea, but hard to formulate,
  - *extra*-core resources, e.g., memory are a challenge; this hints at problem wrt. interface,
  - usability is often overlooked: it's hard to quantify the impact this has,
  - underlying ethos differs somewhat: given the option of

    1. make efficient, *then* make secure
    2. make secure, *then* make efficient

    the latter may be preferable.

Questions?

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