# Bipartite Modular Multiplication 

Marcelo E. Kaihara and<br>Naofumi Takagi

Department of Information Engineering
Nagoya University

## Outline

- Background and Objective
- Preliminaries
- Ordinary Modular Multiplication
- Montgomery Multiplication
- New Method
- Hardware Implementation
- Summary


## Background and Objective

* Modular Multiplication
- Basic operation in public-key cryptographic applications.
- Fast method required
- Operation with large integers (huge amount of computation)
- A fast method enables: The use of large keys and real time decryption.



## Develop fast method for calculating modular multijplication

## Main Idea

## Multiplier is split into two parts

## Ordinary Multiplication

Interleaved
Modular
Multiplication
Algorithm
(classical method)


Montgomery
Multiplication
Montgomery
Multiplication
Algorithm
proposed by
P.L.Montgomery, 1985

## Ordinary Modular Multiplication

Definition:
$M$ : modulus $\quad X, Y \in Z_{M}=\{0,1, \cdots, M-1\}$

$$
X \times Y \triangleq X \cdot Y \bmod M
$$

Multiprecision arithmetic:

$$
r=2^{k}, \quad M=\sum_{i=0}^{n-1} m_{i} \cdot r^{i}, \quad X=\sum_{i=0}^{n-1} x_{i} \cdot r^{i}, Y=\sum_{i=0}^{n-1} y_{i} \cdot r^{i}
$$

## Ordinary Modular Multiplication

Interleaved Modular Multiplication Process of Computation


## Montgomery Multiplication M-Residue System

## Original Residue System

M - Residue System


Chained multiplications (in modular exponentiation) are performed in the M-Residue system

## Montgomery Multiplication

Definition:

$$
\begin{aligned}
& M: n-\operatorname{word}, \operatorname{gcd}(r, M)=1, R_{M}=r^{n}>M \\
& X, Y \in Z_{M}=\{0,1, \cdots, M-1\}
\end{aligned}
$$

$$
X * Y \triangleq X \cdot Y \cdot r^{-n} \bmod M
$$

## Montgomery Multiplication

 Digit-serial Montgomery Algorithm Process of Computation
## Algorithm

A :=X;B := Y; M:= M;
T:=0;
for $\mathrm{i}:=0$ to $\mathrm{n}-1$ do
$\mathrm{T}:=\mathrm{T}+\mathrm{b}_{0} \cdot \mathrm{~A} ;$
$\mathrm{q}_{\mathrm{M}}:=\left(-\mathrm{t}_{0} \cdot \mathrm{~m}_{0}^{-1}\right) \operatorname{modr}$;
$T:=\left(T+q_{M} \cdot M\right) / r ;$
B := B / r;
endfor
if $\mathrm{T} \geq \mathrm{M}$ then $\mathrm{Z}:=\mathrm{T}-\mathrm{M}$;


## New Modular Multiplication

Operands are transformed into a new residue system

## Multiplier is split into two parts

Ordinary
Multiplication
Interleaved
Modular
Multiplication
Algorithm
(classical method)

Process
in parallel
to
boost speed

Montgomery
Multiplication
Montgomery
Multiplication
Algorithm
proposed by
P.L.Montgomery, 1985

## New Modular Multiplication

## A lot of research to speed up both algorithms

## Ordinary <br> Multiplication

Interleaved
Modular
Multiplication
Algorithm
(classical method)


Take advantage of developed techniques


Halve the number of iteration


Double the speed

## New Modular Multiplication

New transformation constant $\mathrm{R}=\mathrm{r}^{\alpha \mathrm{n}}<\mathrm{M}$

$$
\alpha: \alpha \in \mathbb{Q}, 0<\alpha<1, \alpha \cdot n \in Z
$$

Original Residue System
New Residue System

$$
\left(Z_{M}, x\right)
$$

$\left(Z_{M}^{\prime},(8)\right.$
U 4 .............................> $X=U \cdot r^{a n} \bmod M$

Isomorphic
$U \times V=U \cdot V \bmod M \triangleleft \ldots \ldots \ldots \ldots\rangle X \circledast Y=X \cdot Y \cdot r^{-a n} \bmod M$

V 4.............................> $Y=V \cdot r^{a n} \bmod M$

## New Modular Multiplication

## Definition:

$$
\begin{aligned}
& M: n \text { - word, } \operatorname{gcd}(r, M)=1, R=r^{a n}<M \\
& \alpha: \alpha \in \mathbb{Q}, 0<\alpha<1, \alpha \cdot n \in Z \\
& X, Y \in Z_{M}=\{0,1, \cdots, M-1\}
\end{aligned}
$$

$$
X \geqslant Y \triangleq X \cdot Y \cdot r^{-a n} \bmod M
$$

## Computation of the New Modular Multiplication

$$
\begin{aligned}
& X \otimes Y \triangleq X \cdot Y \cdot r^{-\alpha n} \bmod M \\
& Y_{H} \cdot r^{\alpha n}+Y_{L} \\
&= X \cdot\left(Y_{H} \cdot r^{\alpha n}+Y_{L}\right) \cdot r^{-\alpha n} \bmod M \\
&= X \cdot Y_{H} \cdot Y^{\alpha n} \cdot Y^{\alpha n}+X \cdot Y_{L} \cdot r^{-\alpha n} \bmod M \\
&= X \cdot Y_{H}+X \cdot Y_{L} \cdot r^{-\alpha n} \bmod M
\end{aligned}
$$

## Computation of the New Modular Multiplication

## $X \circledast Y=X \cdot Y_{H}+X \cdot Y_{L} \cdot r^{-\alpha n} \bmod M$

Interleaved Modular Multiplication Algorithm

Montgomery Multiplication Algorithm

## New Modular Multiplication

 [Algorithm KT]Input: $\quad \mathrm{M}: \mathrm{r}^{\mathrm{n}-1}<\mathrm{M}<\mathrm{r}^{\mathrm{n}}, \mathrm{M}$ odd

$$
X, Y \in Z_{M}^{\prime}
$$

Output: $Z=X \cdot Y \cdot r^{-a n} \bmod M\left(Z \in Z_{M}^{\prime}\right)$
Algorithm:
Step 1: $A:=X ; M:=M ; S:=0 ; T:=0 ;$

$$
B_{H}:=Y_{H} ; B_{L}:=Y_{L}
$$

Step 2: \{ $\mathrm{S}:=$ Interleaved_ modmul $\left(\mathrm{A}, \mathrm{B}_{\mathrm{H}}\right)$; $\mathrm{T}:=$ Montgomery _ modmul $\left(\mathrm{A}, \mathrm{B}_{\mathrm{L}}\right)$; \}
Step 3: $Z:=(S+T) \bmod M$;

## New Modular Multiplication

 Process of Computation ( $\alpha=1 / 2$ )The multiplier is processed from both sides in parallel

$$
X: Y=X \cdot Y_{H}+X \cdot Y_{L} \cdot r^{-n / 2} \bmod M
$$



## New Modular Multiplication

## Conversions between residue systems

Conversions can be done in half the time
No need for pre-computed constants
Original Residue System
New Residue System


## Hardware Implementation



## Hardware Implementation

From the Original to the New Residue System


## Hardware Implementation

From the New to the Original Residue System


# Hardware Implementation 

## Characteristics of the Circuit Based on the New Algorithm

- Can be constructed using already designed circuits of lower radix.
- Amount of hardware proportional to n.
- When using multipliers of similar performance ( $\alpha=1 / 2$ ), execution time n/2+1 clk cycles, i.e. acceleration twice the speed of the original multipliers.


## Hardware Implementation

Different Combination of Multipliers By changing $\alpha$ it is possible to use different combinations of multipliers


## Summary

- We proposed a new computation method for speeding up modular multiplication. Multiplier processed from both sides in parallel.
- With multipliers of similar performance, number of clock cycles halved. Multipliers of different performance can be used by changing the value of $\alpha$.
* The proposed method suitable for both hardware implementation; and software implementation in a multiprocessor environment.
* The technique used in the proposed method can be adapted for operation in the binary extended field GF(2m).

