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#### New High Entropy Element for FPGA Based True Random Number Generators

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#### - Introduction

- New Entropy Element Design Goals
- Transition Effect Ring Oscillator (TERO)
- Mathematical Model of TERO
- Experimental Results
- Conclusions



Session KeysTemporary KeysSignature ParametersTemporary KeysChallenges for AuthenticationZero Knowledge ProtocolsGeneration of PrimesNonces

...and therefore random numbers must be independent, unpredictable, and must fulfill strict statistical properties.

True Random Number Generators (TRNGs) translate a physical phenomena (e.g. thermal noise) to the random digits.

The TRNG of insufficient quality can weaken an otherwise strong cryptographic system (see e.g. [1]).



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# Introduction Why **True** Random Number Generators?



"Any one who considers arithmetical methods of producing random digits is, of course, in a state of sin. For, as has been pointed out several times, there is no such thing as a random number – there are only methods to produce random numbers, and a strict arithmetic procedure of course is not such a method."

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#### **The Research Challenge:**

To discover such a random source and extraction method, which can be reliably synthesized in modern electronic devices such as Field Programmable Gate Arrays (FPGAs), where cryptographic systems are usually implemeted.

# Introduction FPGA-based TRNG Randomness Sources & Designs

#### **Timing Jitter:**

- of Ring Oscillators (**ROs**):
  - Two **ROs** accompanied with LFSRs (Tkacik; CHES 2002; **compromised** by Dichtl)
  - Fibonacci and Galois **ROs** Combined by XOR (Golic; Tran. on Comp. 2006)
  - 114 ROs combined by XOR (Sunar; Tran. on Comp.; compromised by Dichtl)
  - 20 **ROs** combined by XOR the modification of Sunar's 114 ROs design (Wold, Tan; Int. J. of Reconfig. Comp. 2009; **compromised** by Fischer)
  - The general frequency injection **RO attack** (Markettos, Moore; CHES 2009)
- of PLLs' output (Fischer & Drutarovsky, CHES 2002)

#### **Metastability:**

- Metastable Ring Oscillator (Vasyltsov et.al.; CHES 2008)
  - Authors mentioned difficulties realated to the implementation in FPGA hardware





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Basic RO operation  $t_{1,} t_2$ 

朣

 $\cap$ 

rnd. bit

output

sample

#### **Pros** of the Popular **ROs**:

Basic RO-based TRNG

restart

O

- Employs standard logic cells
- Easy synthesis in FPGAs and ASICs

#### Cons of the Popular ROs:

- Low entropy rate (acquired from internal noise processes in RO electronic components)
- Strong dependence on working conditions and external perturbation
- RO can synchronize on parallel operating ROs or on perturbation









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Starting from simple RO...





...two inverters are replaced by buffers, still the same circuit behavior...





...buffer and inverter are replaced by XORs, which act as buffer and inverter, second buffer is replaced by AND (in order to have the loop symmetric)...





...both XORs can be switched from inverter to buffer logic function simultaneously what can cause oscillations in the circuit if the feedback path is long enough ...





Single CLB Implementation in Xilinx Spartan 3E FPGA and the Oscilloscope Screenshot

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## Transition Effect Ring Oscillator (TERO) LT Spice TERO Circuitry Simulation Result





 $T_{\rm S}$  - width of pulse  $T_{\rm T}$  - period of a when the oscillations are started

single TERO oscillation

 $T_{\rm M}$  - width of pulse when the oscillations disappear

## Transition Effect Ring Oscillator (TERO) LT Spice TERO Circuitry Simulation Result





The shortening of raised pulse plays a crucial role...

- T<sub>S</sub> width of pulse when the oscillations are started
- T<sub>T</sub> period of a single TERO oscillation
- T<sub>M</sub> width of pulse when the oscillations disappear
- $T_{\rm D}$  each oscillation (average) pulse shortening factor

#### Transition Effect Ring Oscillator (TERO) TERO vs. RO comparison using VHDL Macro-Model



VHDL Macro-Model of TERO (and RO - when ctrl = 1' for  $XOR_1$  and ctrl = 0' for  $XOR_2$ )

#### Transition Effect Ring Oscillator (TERO) TERO vs. RO comparison using VHDL Macro-Model



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The ModelSim simulation results of the VHDL structure for both TERO and RO modes





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"Remember that all models are wrong; the practical question is how wrong do they have to be to not be useful."

**George E. P. Box** 



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We need the useful mathematical model in order to:
- show that "randomness" relies on the physical phenomena
- determine how much "randomness" is available
- fulfill TRNG evaluation criteria
- persuade a community on the reliability of a random number generation method




- $T_{\rm T}$  period of a single TERO oscillation
- $T_{\rm S}$  width of pulse when the oscillations are started
- $T_{\rm M}$  width of pulse when the oscillations disappear
- T<sub>D</sub> each oscillation (average) pulse shortening factor
- $\Delta_{T_{ij}}$  period jitter or instability of shortening factor
- Y<sub>Tj</sub> number of oscillations done each *j*-th ctrl period





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mean value of number of oscs. in **TERO mode** 

$$\overline{Y_{\rm T}} \approx \frac{T_{\rm S} - T_{\rm M}}{T_{\rm D}}$$

std. deviation of number of oscs. in **TERO mode** 

$$\sigma_{Y_{\rm T}} \approx \frac{\sigma}{T_{\rm D}} \sqrt{\overline{Y_{\rm T}}}$$

where  $\sigma$  is std. deviation of a period jitter



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mean value of number of oscs. in **RO mode** 

$$\overline{Y_{\rm R}} \approx \frac{T_{\rm nrst}}{2T_{\rm T}}$$

where  $T_{nrst}$  is time when RO is oscillating

std. deviation of number of oscs. in **RO mode** 





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std. deviation of number of oscs. in TERO mode



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std. deviation of number of oscs.  $\sigma_{\gamma_R} \approx \frac{\sigma}{2T_T}$ in RO mode



$$\frac{\sigma_{Y_{\rm T}}}{\sigma_{Y_{\rm R}}} \approx \frac{2T_{\rm T}}{T_{\rm D}} \sqrt{\frac{2T_{\rm T} \left(T_{\rm S} - T_{\rm M}\right)}{T_{\rm D} T_{\rm nrst}}} \approx$$



mean value of number of oscs. in **TERO mode** 

$$\overline{Y_{\rm T}} \approx \frac{T_{\rm S} - T_{\rm M}}{T_{\rm D}}$$

mean value of number of oscs. in **RO mode** 

≈ 100 ~ 500 !!!

 $\frac{\sigma_{Y_{\rm T}}}{\sigma_{Y_{\rm R}}} \approx -$ 

$$\overline{Y_{\rm R}} \approx \frac{I_{\rm nrst}}{2T_{\rm T}}$$

 $\frac{2T_{\rm T}(T_{\rm S}-T_{\rm M})}{T_{\rm T}T_{\rm T}}\approx$ 

where  $T_{nrst}$  is time when RO is oscillating





Matlab simulation of TERO and RO math. models





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Evaluation Platform implemented in Xilinx Spartan 3E FPGA





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TERO Place & Route detail, where each channel is implemented in separated CLB





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Two mutual TERO compositions: Next and Diagonal used in practical experiments





The **comparison** of number of oscillations for both **TERO** and **RO modes** 

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The **comparison** of normalized autocorrelation of number of oscillations (LSB) for both **TERO** and **RO modes** 











TEST	Source	Next(TERO)	Diag.(TERO)	Next(RO)	Diag.(RO)
Mean	LSB A / LSB B	0.51/0.48	0.51/0.48	0.47/0.44	0.55/0.46
Value	LSB(A XOR B)	0.5002	0.4999	0.4539	0.7926
Normalized					
cross-correlation	LSB (A,B)	0.4160	-0.0917	-94.3378	599.3945
(for shift= $0$ )					
NIST / FIPS	Only LSB A	F / P	F / F	- / F	- / F
Statistical	Only LSB B	F / F	F / F	- / F	- / F
tests result	LSB(A XOR B)	P / P	P / P	- / F	- / F





















TERO structure adapted for Actel Fusion FPGA



Evaluation Platform implemented in Actel Fusion FPGA





Histograms of number of TERO oscillations of all 16 TERO channels; Placement #1



Histograms of number of TERO oscillations of all 16 TERO channels; Placement #2





Histograms of number of TERO oscillations of a single TERO channel under variously violated working conditions





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- New entropy element (TERO) introduced
- High sensitivity to random processes inside FPGA logic cells, while rejecting global perturbation
- Inner testability counting of number of oscillations
- Basic mathematical model was introduced
- Two XOR-combined TERO channels can pass the NIST 800-22 statistical tests
- Speed from 100kpbs to 250 kbps per single TRNG
- Stateless entropy concept
- Performance of TEROs cluster appears to be independent from the position in FPGA and from implementation in another identical FPGA board, and from working conditions



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"We would like to thank Actel University Program for a donation of 10 Actel Fusion FPGA evaluation boards, which enabled us to confirm the TERO principle using number of identical FPGA boards."
## Thank You for the Attention